

1/3-Inch 1.3Mp SOC Digital Image Sensor Die

MT9M111

For the product data sheet, refer to Aptina's Web site: www.aplina.com

Features

- Aptina[®] DigitalClarity[®] CMOS imaging technology
- System-on-a-chip (SOC)—Completely integrated camera system
- Ultra low-power, low-cost, progressive scan CMOS image sensor
- On-die image flow processor (IFP) performs sophisticated processing: color recovery and correction, sharpening, gamma, lens shading correction, and on-the-fly defect correction
- Filtered image downscaling to arbitrary size with smooth, continuous zoom and pan
- Automatic features: auto exposure, auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, auto defect identification and correction
- Fully automatic xenon and LED-type flash support including fast exposure adaptation
- Multiple parameter contexts for easy/fast mode switching
- Camera control sequencer that automates snapshots, snapshots with flash, and video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB
- Output FIFO and integer clock divider: “uniform” pixel clocking

General Physical Specifications

- Die thickness: 305 μ m \pm 12 μ m (12.0 mil \pm 0.5 mil)
Wafer thickness: 750 μ m \pm 25 μ m
(Consult factory for die thickness other than 305 μ m)
- Backside wafer surface of bare silicon
- Typical metal 1 thickness: 3.1k Å
- Typical metal 2 thickness: 3.1k Å
- Typical metal 3 thickness: 6.1k Å
- Metallization composition: 99.5 percent Al and 0.5 percent Cu over Ti
- Typical topside passivation:
2.2k Å nitride over 6.0k Å of undoped oxide
- Passivation openings (MIN): 75 μ m x 90 μ m

Order Information

Wafer: MT9M111W00STCK14LC1

Die: MT9M111D00STCK14LC1

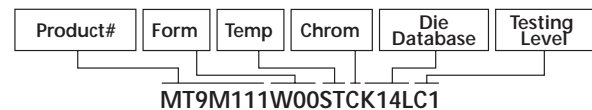
Die Database

- Die outline, see Figure 2 on page 9
- Die size (stepping interval): 7,481.80 μ m x 7,370.00 μ m
- Singulated die size:
7,440 μ m \pm 25 μ m x 7,328 μ m \pm 25 μ m
- Bond Pad Location and Identification Tables, see pages 5–8

Option

- Form
 - Die D
 - Wafer W
- Testing
 - Standard (level 1) probe C1

Notes: 1. Please consult die distributor or factory before ordering to verify long-term availability of these die products.



Key Performance Parameters

- Optical format: 1/3-inch (5:4)
- Active imager size: 4.61mm(H) x 3.69mm(V), 5.90mm diagonal
- Active pixels: 1,280H x 1,024V
- Pixel size: 3.6 μ m x 3.6 μ m
- Maximum data rate/maximum master clock:
27 MPS/54 MHz
- Frame rate: SXGA (1,280H x 1,024V) 15 fps at 54 MHz
QSXGA (640H x 512V) 30 fps at 54 MHz
- ADC resolution: 10-bit, dual on-die
- Responsivity: 1.0 V/lux-sec (550nm)
- Dynamic range: 71dB
- SNR_{MAX}: 44dB
- Supply voltage: I/O digital 1.7–3.1V
Core digital 2.5–3.1V (2.8V nominal)
Analog 2.5–3.1V (2.8V nominal)
- Power consumption:
170mW SXGA at 15 fps (54 MHz CLKIN)
90mW QSXGA at 30 fps (54 MHz low-power mode)
- Operating temperature, T_A: –30°C to +70°C

General Description

The Aptina Imaging MT9M111 die is an SXGA-format single-chip camera with a one-third-inch CMOS active-pixel digital image sensor. This device combines the MT9M011 image sensor core with fourth-generation digital-image-flow processor technology from Aptina Imaging. It captures high quality color images at SXGA resolution.

The MT9M111 die features DigitalClarity—Aptina’s breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor is a complete camera-on-a-chip solution designed specifically to meet the low-power, lowcost demands of battery-powered products such as cellular phones, PDAs, and toys. It incorporates sophisticated camera functions on-die and is programmable through a simple two-wire serial interface.

The MT9M111 die performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure (AE), automatic 50Hz/60Hz flicker avoidance, lens-shading correction, auto white balance (AWB), and on-the-fly defect identification and correction. Additional features include day/night mode configurations; special camera effects such as sepia tone and solarization; and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both xenon and LED-type flash light sources in several snapshot modes.

The MT9M111 die can be programmed to output progressive-scan images up to 30 frames per second (fps) in preview power-saving mode, and 15 fps in full-resolution (SXGA) mode. In either mode, the image data can be output in any one of six 8-bit formats:

- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- “Processed” Bayer

The FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Die Testing Procedures

Aptina imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to test product functionality in Aptina’s standard package. Because the package environment is not within Aptina’s control, the user must determine the necessary heat-sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die analog-to-digital converter (ADC), logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data. Aptina retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. Aptina reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to Aptina's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided here are for reference only. For target functional and parametric specifications, refer to the packaged product data sheet found on Aptina's Web site.

Bonding Instructions

The MT9M111 imager die has 51 bond pads. Refer to Tables 1 and 2 for a complete list of bond pads and coordinates.

The MT9M111 imager die does not require the user to determine bond option features.

The MT9M111 imager die also has several pads defined as "do not use." These pads are used for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 on page 4 shows the MT9M111 typical die connections. For low-noise operation the MT9M111 die requires separate supplies for analog and digital power. Incoming digital and analog ground conductors can be tied together right next to the die. Both power supply rails should be decoupled to ground using ceramic capacitors. The use of inductance filters is not recommended.

The MT9M111 imager die also supports different digital core (VDD/DGND) and I/O power (VDDQ/DGNDQ) power domains that can be at different voltages.

Wafer Saw

The die size (stepping interval) provided is measured from the center of the die street on one side of the die to the center of the die street on the other side of the die. A singulated die is approximately $42\mu\text{m}$ smaller in length and width. The dimensional tolerance of a singulated die is $\pm 25\mu\text{m}$. For example, if the die width (stepping interval) is $5,080\mu\text{m}$ and the die length (stepping interval) is $7,620\mu\text{m}$, the dimensions of the singulated die will be $5,038\mu\text{m} \pm 25\mu\text{m}$ by $7,578\mu\text{m} \pm 25\mu\text{m}$.

Wafer-Level Processing

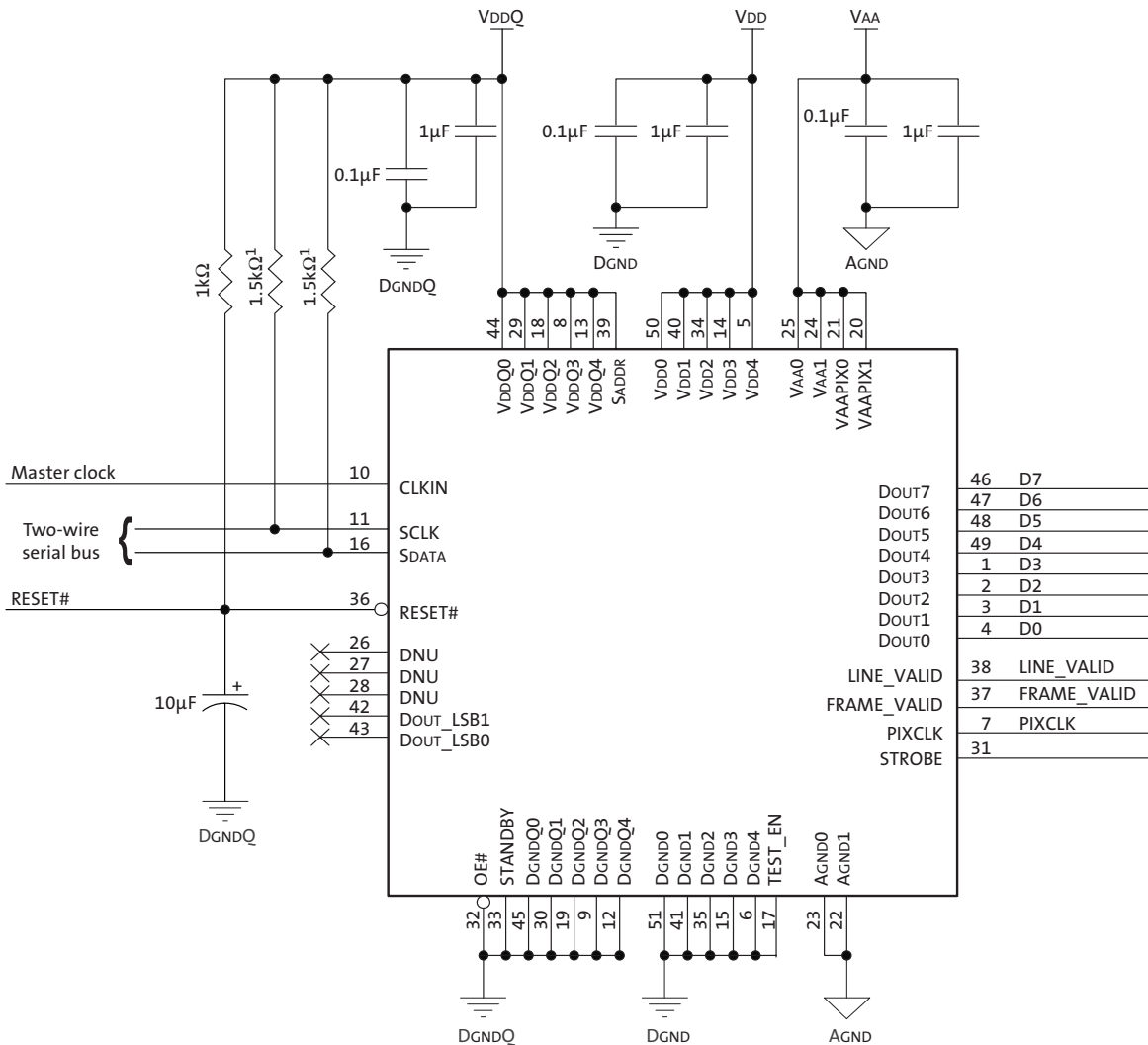
Customers should choose the wafer form when post-processing of die is required. This includes adding extra passivation or metal layers or bumping of the bond pads. For these customers, the street widths are provided in the die outline. Also, a reference from the center of bond pad 1 to the center of the intersection of two streets is provided for easy alignment.

Storage Requirements

Aptina die products are packaged for shipping in a cleanroom environment. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage. Aptina recommends the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should

be maintained at 30 percent relative humidity ± 10 percent. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Figure 1: Typical Configuration (Connection)



- Notes:
1. A 1.5k Ω resistor value is recommended, but a greater value may be for slower two-wire speed.
 2. VDD, VAA, VAAPIX must all be at the same potential, though if connected, care must be taken to avoid excessive noise injection into the VAA/VAAPIX power domains.

Bond Pad Location and Identification Tables

Table 1: MT9M111 Bond Pad Location and Identification from Center of Pad 1

Pad	MT9M111	"X" ¹ Microns	"Y" ¹ Microns	"X" ¹ Inches	"Y" ¹ Inches
1	DOUT3	0.00	0.00	0.0000000	0.0000000
2	DOUT2	466.56	0.00	0.0183685	0.0000000
3	DOUT1	933.12	0.00	0.0367370	0.0000000
4	DOUT0	1399.68	0.00	0.0551055	0.0000000
5	VDD4	2099.52	0.00	0.0826583	0.0000000
6	DGND4	2566.08	0.00	0.1010268	0.0000000
7	PIXCLK	3265.92	0.00	0.1285795	0.0000000
8	VDDQ3	3965.76	0.00	0.1561323	0.0000000
9	DGNDQ3	4432.32	0.00	0.1745008	0.0000000
10	CLKIN	5132.16	0.00	0.2020535	0.0000000
11	SCLK	5598.72	0.00	0.2204220	0.0000000
12	DGNDQ4	6065.28	0.00	0.2387906	0.0000000
13	VDDQ4	6707.19	-715.45	0.2640624	-0.0281671
14	VDD3	6707.19	-1182.01	0.2640624	-0.0465356
15	DGND3	6707.19	-1648.57	0.2640624	-0.0649041
16	SDATA	6707.19	-2115.13	0.2640624	-0.0832726
17	TEST_EN	6707.19	-2581.69	0.2640624	-0.1016411
18	VDDQ2	6707.19	-3048.25	0.2640624	-0.1200096
19	DGNDQ2	6707.19	-3514.81	0.2640624	-0.1383781
20	VAAPIX1	6707.19	-4082.17	0.2640624	-0.1607152
21	VAAPIX0	6707.19	-4548.73	0.2640624	-0.1790837
22	AGND1	6707.19	-5283.13	0.2640624	-0.2079970
23	AGND0	6707.19	-5749.69	0.2640624	-0.2263656
24	VAA1	6707.19	-6216.25	0.2640624	-0.2447341
25	VAA0	6707.19	-6682.81	0.2640624	-0.2631026
26	DNU ²	5948.40	-7019.11	0.2341890	-0.2763429
27	DNU	5481.84	-7019.11	0.2158205	-0.2763429
28	DNU	5015.28	-7019.11	0.1974520	-0.2763429
29	VDDQ1	4344.80	-7019.11	0.1710551	-0.2763429
30	DGNDQ1	3878.24	-7019.11	0.1526866	-0.2763429
31	STROBE	3178.40	-7019.11	0.1251339	-0.2763429
32	OE#	2711.84	-7019.11	0.1067654	-0.2763429
33	STANDBY	2245.28	-7019.11	0.0883969	-0.2763429
34	VDD2	1778.72	-7019.11	0.0700283	-0.2763429
35	DGND2	1312.16	-7019.11	0.0516598	-0.2763429
36	RESET#	845.60	-7019.11	0.0332913	-0.2763429
37	FRAME_VALID	379.04	-7019.11	0.0149228	-0.2763429
38	LINE_VALID	-87.52	-7019.11	-0.0034457	-0.2763429
39	SADDR	-423.83	-6595.29	-0.0166860	-0.2596569
40	VDD1	-423.83	-6128.73	-0.0166860	-0.2412884
41	DGND1	-423.83	-5662.17	-0.0166860	-0.2229199
42	DOUT_LSB1	-423.83	-5195.61	-0.0166860	-0.2045514
43	DOUT_LSB0	-423.83	-4729.05	-0.0166860	-0.1861829

Table 1: MT9M111 Bond Pad Location and Identification from Center of Pad 1 (continued)

Pad	MT9M111	"X"1 Microns	"Y"1 Microns	"X"1 Inches	"Y"1 Inches
44	VDDQ0	-423.83	-4029.21	-0.0166860	-0.1586301
45	DGNDQ0	-423.83	-3562.65	-0.0166860	-0.1402616
46	DOUT7	-423.83	-2862.81	-0.0166860	-0.1127089
47	DOUT6	-423.83	-2396.25	-0.0166860	-0.0943404
48	DOUT5	-423.83	-1929.69	-0.0166860	-0.0759719
49	DOUT4	-423.83	-1463.13	-0.0166860	-0.0576033
50	VDD0	-423.83	-996.57	-0.0166860	-0.0392348
51	DGND0	-423.83	-530.01	-0.0166860	-0.0208663

- Notes:
1. Reference to center of each bond pad from center of bond pad 1.
 2. DNU = "Do not use."

Table 2: MT9M111 Bond Pad Location and Identification from Center of Die (0,0)

Pad	MT9M111	"X"1 Microns	"Y"1 Microns	"X"1 Inches	"Y"1 Inches
1	DOUT3	-3141.68	3509.56	-0.1236882	0.1381715
2	DOUT2	-2675.12	3509.56	-0.1053197	0.1381715
3	DOUT1	-2208.56	3509.56	-0.0869512	0.1381715
4	DOUT0	-1742.00	3509.56	-0.0685827	0.1381715
5	VDD4	-1042.16	3509.56	-0.0410299	0.1381715
6	DGND4	-575.60	3509.56	-0.0226614	0.1381715
7	PIXCLK	124.24	3509.56	0.0048913	0.1381715
8	VDDQ3	824.08	3509.56	0.0324441	0.1381715
9	DGNDQ3	1290.64	3509.56	0.0508126	0.1381715
10	CLKIN	1990.48	3509.56	0.0783654	0.1381715
11	SCLK	2457.04	3509.56	0.0967339	0.1381715
12	DGNDQ4	2923.60	3509.56	0.1151024	0.1381715
13	VDDQ4	3565.51	2794.11	0.1403742	0.1100043
14	VDD3	3565.51	2327.55	0.1403742	0.0916358
15	DGND3	3565.51	1860.99	0.1403742	0.0732673
16	SDATA	3565.51	1394.43	0.1403742	0.0548988
17	TEST_EN	3565.51	927.87	0.1403742	0.0365303
18	VDDQ2	3565.51	461.31	0.1403742	0.0181618
19	DGNDQ2	3565.51	-5.25	0.1403742	-0.0002067
20	VAAPIX1	3565.51	-572.61	0.1403742	-0.0225437
21	VAAPIX0	3565.51	-1039.17	0.1403742	-0.0409122
22	AGND1	3565.51	-1773.57	0.1403742	-0.0698256
23	AGND0	3565.51	-2240.13	0.1403742	-0.0881941
24	VAA1	3565.51	-2706.69	0.1403742	-0.1065626
25	VAA0	3565.51	-3173.25	0.1403742	-0.1249311
26	DNU ²	2806.72	-3509.56	0.1105008	-0.1381715
27	DNU	2340.16	-3509.56	0.0921323	-0.1381715
28	DNU	1873.60	-3509.56	0.0737638	-0.1381715
29	VDDQ1	1203.12	-3509.56	0.0473669	-0.1381715
30	DGNDQ1	736.56	-3509.56	0.0289984	-0.1381715
31	STROBE	36.72	-3509.56	0.0014457	-0.1381715
32	OE#	-429.84	-3509.56	-0.0169228	-0.1381715
33	STANDBY	-896.40	-3509.56	-0.0352913	-0.1381715
34	VDD2	-1362.96	-3509.56	-0.0536598	-0.1381715
35	DGND2	-1829.52	-3509.56	-0.0720283	-0.1381715
36	RESET#	-2296.08	-3509.56	-0.0903969	-0.1381715
37	FRAME_VALID	-2762.64	-3509.56	-0.1087654	-0.1381715
38	LINE_VALID	-3229.20	-3509.56	-0.1271339	-0.1381715
39	SADDR	-3565.51	-3085.73	-0.1403742	-0.1214854
40	VDD1	-3565.51	-2619.17	-0.1403742	-0.1031169
41	DGND1	-3565.51	-2152.61	-0.1403742	-0.0847484
42	DOUT_LSB1	-3565.51	-1686.05	-0.1403742	-0.0663799
43	DOUT_LSB0	-3565.51	-1219.49	-0.1403742	-0.0480114
44	VDDQ0	-3565.51	-519.65	-0.1403742	-0.0204587
45	DGNDQ0	-3565.51	-53.09	-0.1403742	-0.0020902

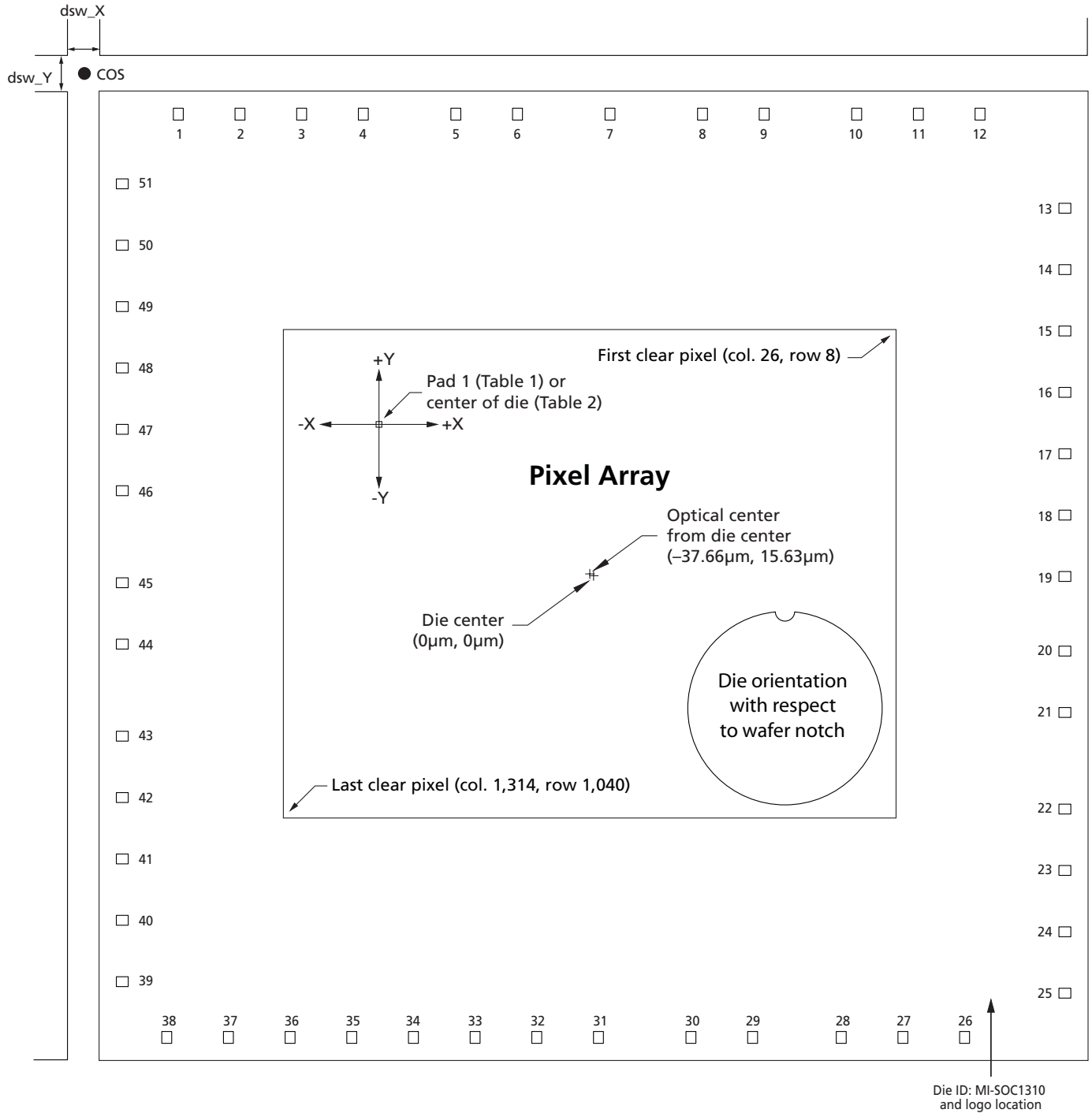
Table 2: MT9M111 Bond Pad Location and Identification from Center of Die (0,0) (continued)

Pad	MT9M111	"X"1 Microns	"Y"1 Microns	"X"1 Inches	"Y"1 Inches
46	DOUT7	-3565.51	646.75	-0.1403742	0.0254626
47	DOUT6	-3565.51	1113.31	-0.1403742	0.0438311
48	DOUT5	-3565.51	1579.87	-0.1403742	0.0621996
49	DOUT4	-3565.51	2046.43	-0.1403742	0.0805681
50	VDD0	-3565.51	2512.99	-0.1403742	0.0989366
51	DGND0	-3565.51	2979.55	-0.1403742	0.1173051

- Notes: 1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = "Do not use."

Die Features

Figure 2: Die Outline (Top View)



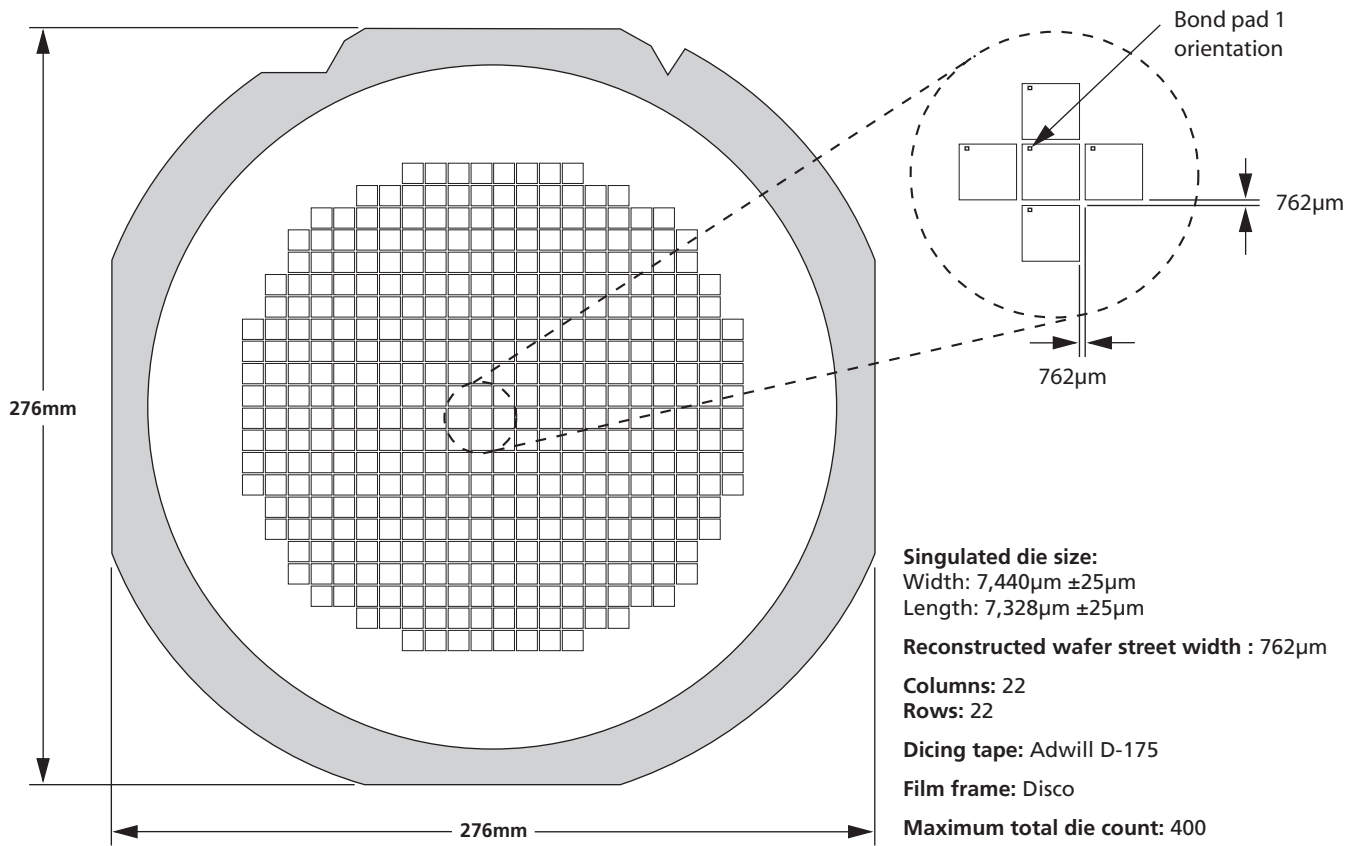
Notes: 1. Die street widths are not drawn to scale. Die outline shows streets and bond pads passivation openings.

Physical Specifications

Table 3: Physical Dimensions

Feature	Dimensions
Wafer diameter	200mm (8in)
Die thickness	305 μ m \pm 12 μ m (12.0 mil \pm 0.5 mil)
Wafer thickness	750 μ m \pm 25 μ m
Die size (stepping interval):	7,481.80 μ m x 7,370.00 μ m (294.559 mil x 290.157 mil)
Singulated die size Width (X dimension): Length (Y dimension):	7,440 μ m \pm 25 μ m 7,328 μ m \pm 25 μ m
Street width along X-axis (dsw_x)	127.0 μ m (5.00 mil)
Street width along Y-axis (dsw_y)	127.0 μ m (5.00 mil)
Center of streets (COS) (relative to center of bond pad 1)	X = -599.22 μ m, Y = 175.06 μ m (X = -23.591 mil, Y = 6.892 mil)
Bond pad size (MIN)	85 μ m x 100 μ m (3.35 mil x 3.94 mil)
Passivation openings (MIN)	75 μ m x 90 μ m (2.95 mil x 3.54 mil)
Minimum bond pad pitch	466.56 μ m (18.369 mil)
Optical array Optical center from die center:	-37.66 μ m, Y = 15.63 μ m
First clear pixel (col. 28, row 8) From die center: From center of pad 1:	X = 2,280.51 μ m, Y = 1,873.39 μ m X = 5,422.19 μ m, Y = -1,636.17 μ m
Last clear pixel (col. 1,314, row 1,040) From die center: From center of pad 1:	X = -2,356.16 μ m, Y = -1,841.76 μ m X = 785.52 μ m, Y = -5,351.31 μ m
Die offset From center of wafer to center of die (wafer notch at bottom):	X = 0.00000mm, Y = -3.65500mm

Figure 3: MT9M111 Die Orientation in Reconstructed Wafer



Revision History

Rev. J.....		4/10
	<ul style="list-style-type: none"> • Updated to non-confidential 	
Rev. I.....		5/7/09
	<ul style="list-style-type: none"> • Updated to Aptina template • Updated Figure 1: “Typical Configuration (Connection),” on page 4, • Updated Table 1 on page 5 <ul style="list-style-type: none"> – Renamed pin 17 to TEST_EN – Renamed pin 42 to DOUT_LSB1 – Renamed pin 43 to DOUT_LSB0 • Updated Table 2 on page 7 <ul style="list-style-type: none"> – Renamed pin 17 to TEST_EN – Renamed pin 42 to DOUT_LSB1 – Renamed pin 43 to DOUT_LSB0 	
Rev H.....		4/07
	<ul style="list-style-type: none"> • Updated to new format • Added DigitalClarity to trademarks 	
Rev G.....		2/06
	<ul style="list-style-type: none"> • Added die offset information to Table 3 on page 10 • Added 750µm ±25µm wafer thickness to pages 1 and 10 	
Rev F.....		6/05
	<ul style="list-style-type: none"> • Changed I/O digital supply voltage from 1.7V–3.6V to 1.7V–3.1V 	
Rev E.....		5/05
	<ul style="list-style-type: none"> • Added singulated die size • Updated text for “Wafer Saw” on page 3 • Updated template 	
Rev D.....		9/04
	<ul style="list-style-type: none"> • Removed Preliminary data sheet designation • Updated Automatic Features text on page 1 • Added “stepping interval” to “Order Information” on page 1 • Updated Figure 1 on page 4 • Updated pad names in Table 1 on page 5 and Table 2 on page 7 • Updated Figure 2 on page 9 • Removed note 2 from page 9 • Updated coordinates • Updated optical center, first clear pixel and last clear pixel X coordinates on pages 9 and 10 • Updated first and last clear pixel column information on pages 9 and 10 	
Rev C, Preliminary.....		6/04
	<ul style="list-style-type: none"> • Update document title • Added two bullets to Features section on page 1 • Updated Supply Voltage, and Operating temperature specifications on page 1 • Updated General Description and Bonding Instructions text 	

	<ul style="list-style-type: none"> Updated Figure 1 	
Rev B, Preliminary	4/04
	<ul style="list-style-type: none"> Added Figure 3 on page 11 	
Rev A, Preliminary	3/04
	<ul style="list-style-type: none"> Initial release 	

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 This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final,
 these specifications are subject to change, as further product development and data characterization sometimes occur.