MODEL NAME : LA-F371P non-AR
PCB NO : DAA000EC010
BOM P/N : 431A8C31L01

Dell/Compal Confidential

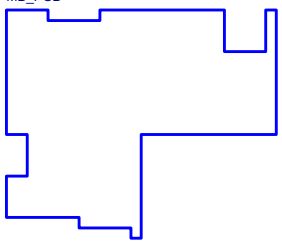
Schematic Document

Pebble Creek MLK (Kabylake R/U)

2017-11-03

Rev: 1.0

ZZZ
MB_PCB



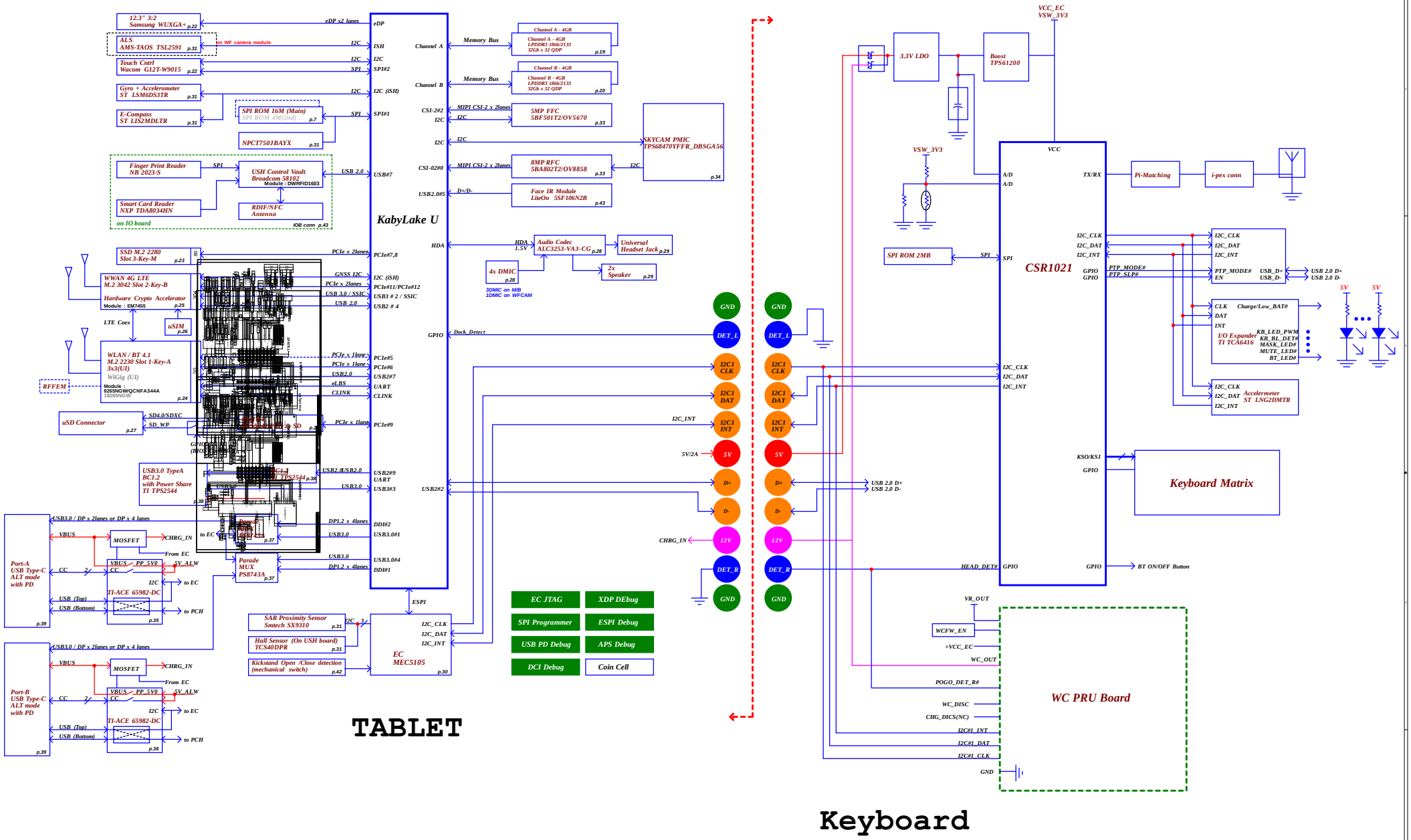
Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

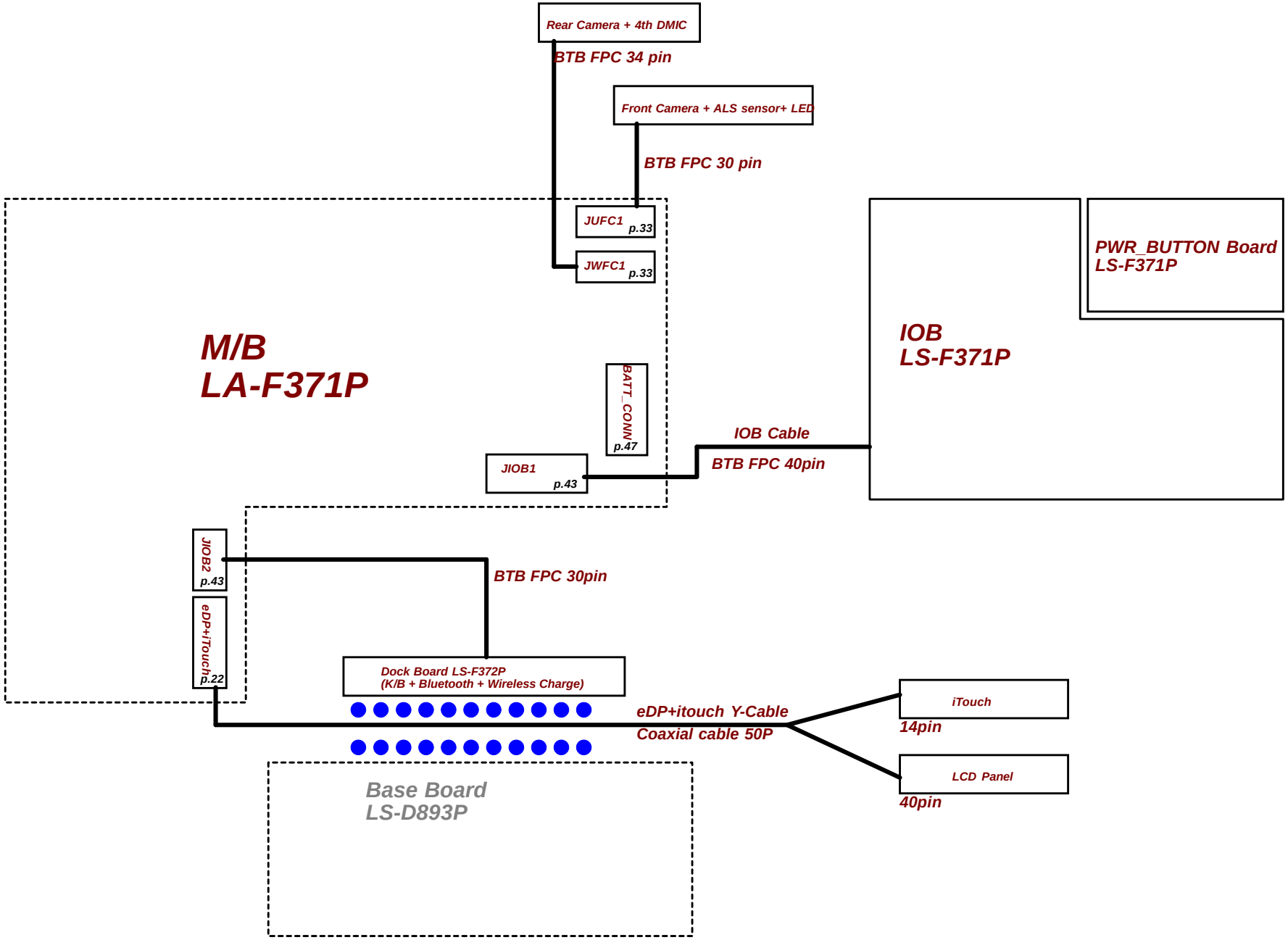
Title: P01-Cover Page

Size | Document Number: LA-F371P | Rev: 1.0

Date: Tuesday, November 07, 2017 | Sheet 1 of 65



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/03/20	Deciphered Date	2015/03/20
			P02-Block Diagram
			LA-F371P
			Rev 1.0



Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P03-DaughterB block diagram

Size	Document Number	Rev
	LA-F371P	1.0

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Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	REV	
0	240K +/- 5%	4700p		
1	130K +/- 5%	4700p	Pre-EVT1	
2	62K +/- 5%	4700p	EVT1	
3	33K +/- 5%	4700p	DVT1	
4	8.2K +/- 5%	4700p	DVT2	
5	4.3K +/- 5%	4700p	PVT	
6	2K +/- 5%	4700p		
7	NC			

Board ID Table

Board ID	PCB Revision
0	
1	0.1
2	0.2
3	0.3
4	0.4
5	1.0
6	
7	

USB 3.0

Flexible I/O	Interface	DESTINATION
1	USB 3.0 #1	USB Type-C Port-A
2	USB 3.0 #2/SSIC	NGFF (WWAN)
3	USB 3.0 #3	USB 3.0 Type-A
4	USB 3.0 #4	USB Type-C Port-B
5	PCI-E#1 / USB 3.0#5	Reserved for AR
6	PCI-E#2 / USB 3.0#6	Reserved for AR
7	PCI-E #3	Reserved for AR
8	PCI-E #4	Reserved for AR
9	PCI-E #5	NGFF (WLAN)
10	PCI-E #6	
11	PCI-E #7	NGFF (SSD)
12	PCI-E #8 /SATA #1	NGFF (SSD) #7/#8 2lane PCI-E
13	PCI-E #9	Card Reader
14	PCI-E #10	
15	PCI-E #11	NGFF (WWAN/2nd SSD)
16	PCI-E #12	NGFF (WWAN/2nd SSD)

SMBUS Control Table

	SOURCE	Base	BATT	Charger	XDP	USH	PD Controller	Trinity Dock	P-Sensor	MUX	IMVP	IO EXpendor
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
SMBCLK SMBDATA	PCH				V							
EC_SMB00_CLK EC_SMB00_DAT	MEC5105					V	V			V		
EC_SMB01_CLK EC_SMB01_DAT	MEC5105										V	
EC_SMB02_CLK EC_SMB02_DAT	MEC5105			V								V
EC_SMB03_CLK EC_SMB03_DAT	MEC5105											
EC_SMB04_CLK EC_SMB04_DAT	MEC5105						V		V	V		
EC_SMB05_CLK EC_SMB05_DAT	MEC5105	V						V				
EC_SMB10_CLK EC_SMB10_DAT	MEC5105		V									

No use

Link

Port Mapping USB 2.0 CLK

USB 2.0 PORT#	DESTINATION
1	Type-C Port-A
2	Dock
3	Type-C Port-B
4	WWAN
5	IR CAM
7	WLAN
9	USB Type-A
10	USH

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	
	CLKOUT_PCIE1	NGFF (WLAN)
	CLKOUT_PCIE2	NGFF (WWAN)
	CLKOUT_PCIE3	SSD
	CLKOUT_PCIE5	Card Reader
	FLEX CLOCKS	DESTINATION
	CLKOUT_LPC_0	ESPI
	CLKOUT_LPC_1	ESPI

Displayport

	DDI PORT#	DESTINATION
DDI	1	USB Type-C Port-B
	2	USB Type-C Port-A

Symbol Note :

@ : means de-pop

: means Digital Ground

: means Analog Ground

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P04-Notes List

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Functional Strap Definitions
GPP_E19 (Internal Pull Down): DDPB_CTRLDATA
0 = Port B is not detected.
1 = Port B is detected.
GPP_E21 (Internal Pull Down): DDPC_CTRLDATA
0 = Port C is not detected.
1 = Port C is detected.

Type-C PortB

Type-C PortA

@UCPU1A SKL-U

2Lane eDP

COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils, Isolat i on Spad ng=25 mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0

4+2 CPU Option

2+2 CPU Option

@UCPU1I SKL_ULT

DDR Memory Configurati no Type Strappin

GPIO Pin	Pin Name		Micron 8G	Micron 16G	Micron 32G	Hynix 8G	Hynix 16G	Hynix 32G	Samsung 8G	Samsung 16G	Samsung 32G		Micron 32G	Hynix 32G	Samsung 32G	Micron 16G	Hynix 16G	Samsung 16G
GPP_F13	MEM_CONFIG0		0	1	0	1	0	1	0	1	0		1	0	1	0	1	0
GPP_F14	MEM_CONFIG1		0	0	1	1	0	0	1	1	0		0	1	1	0	0	1
GPP_F15	MEM_CONFIG2	1866Mbps	0	0	0	0	1	1	1	1	0	2133Mbps	0	0	0	1	1	1
GPP_F16	MEM_CONFIG3		0	0	0	0	0	0	0	0	1		1	1	1	1	1	1

X76 DRAM Option (R1) , R3 check P08

DRAM Config Option

(Resistor pop location)

MEM_CONFIG0 MEM_CONFIG1 MEM_CONFIG2 MEM_CONFIG3

X7669231L05	Micron 8G/1866	MICRON_8G@ UD1 MT52L256M32D1PF-107WT SA00009XU0L; MICRON_8G@ UD2 MT52L256M32D1PF-107WT SA00009XU0L; MICRON_8G@ UD3 MT52L256M32D1PF-107WT SA00009XU0L; MICRON_8G@ UD4 MT52L256M32D1PF-107WT SA00009XU0L
X7669231L07	Micron 16G/1866	MICRON_16G@ UD1 MT52L512M32D2PF-107WT SA00009U70L; MICRON_16G@ UD2 MT52L512M32D2PF-107WT SA00009U70L; MICRON_16G@ UD3 MT52L512M32D2PF-107WT SA00009U70L; MICRON_16G@ UD4 MT52L512M32D2PF-107WT SA00009U70L
X7669231L09	Micron 32G/1866	MICRON_32G@ UD1 MT52L1G32D4PG-107WT SA00009XV0L; MICRON_32G@ UD2 MT52L1G32D4PG-107WT SA00009XV0L; MICRON_32G@ UD3 MT52L1G32D4PG-107WT SA00009XV0L; MICRON_32G@ UD4 MT52L1G32D4PG-107WT SA00009XV0L
X7669231L06	Hynix 8G/1866	HYNIX_8G@ UD1 H9CCNNN8GTMLAR-NUD FBGA SA00008G64L; HYNIX_8G@ UD2 H9CCNNN8GTMLAR-NUD FBGA SA00008G64L; HYNIX_8G@ UD3 H9CCNNN8GTMLAR-NUD FBGA SA00008G64L; HYNIX_8G@ UD4 H9CCNNN8GTMLAR-NUD FBGA SA00008G64L
X7669231L08	Hynix 16G/1866	HYNIX_16G@ UD1 H9CCNNNBJTMLAR-NUD FBGA SA00008FJ4L; HYNIX_16G@ UD2 H9CCNNNBJTMLAR-NUD FBGA SA00008FJ4L; HYNIX_16G@ UD3 H9CCNNNBJTMLAR-NUD FBGA SA00008FJ4L; HYNIX_16G@ UD4 H9CCNNNBJTMLAR-NUD FBGA SA00008FJ4L
X7669231L10	Hynix 32G/1866	HYNIX_32G@ UD1 H9CCNNNCLTMLAR-NUD FBGA SA0000AEN0L; HYNIX_32G@ UD2 H9CCNNNCLTMLAR-NUD FBGA SA0000AEN0L; HYNIX_32G@ UD3 H9CCNNNCLTMLAR-NUD FBGA SA0000AEN0L; HYNIX_32G@ UD4 H9CCNNNCLTMLAR-NUD FBGA SA0000AEN0L
X7669231L01	Samsung 8G/1866	X76_8G@ X768G X76 X7669231L01; SAMSUNG_8G@ UD1 K4E8E324EB-EGCF FBGA178 SA00009XY0L; SAMSUNG_8G@ UD2 K4E8E324EB-EGCF FBGA178 SA00009XY0L; SAMSUNG_8G@ UD3 K4E8E324EB-EGCF FBGA178 SA00009XY0L; SAMSUNG_8G@ UD4 K4E8E324EB-EGCF FBGA178 SA00009XY0L
X7669231L02	Samsung 16G/1866	X76_16G@ X7616G X76 X7669231L02; SAMSUNG_16G@ UD1 K4E6E304EB-EGCF FBGA17 SA00008QV2L; SAMSUNG_16G@ UD2 K4E6E304EB-EGCF FBGA17 SA00008QV2L; SAMSUNG_16G@ UD3 K4E6E304EB-EGCF FBGA17 SA00008QV2L; SAMSUNG_16G@ UD4 K4E6E304EB-EGCF FBGA17 SA00008QV2L
X7669231L03	Samsung 32G/1866	X76_32G@ X7632G X76 X7669231L03; SAMSUNG_32G@ UD1 4EBE304EB-EGCF FBGA178 SA00008X10L; SAMSUNG_32G@ UD2 4EBE304EB-EGCF FBGA178 SA00008X10L; SAMSUNG_32G@ UD3 4EBE304EB-EGCF FBGA178 SA00008X10L; SAMSUNG_32G@ UD4 4EBE304EB-EGCF FBGA178 SA00008X10L

X76_M8G@ RH18 10K_0402_5% SD028100280	X76_M8G@ RH16 10K_0402_5% SD028100280	X76_M8G@ RH13 10K_0402_5% SD028100280	X76_M8G@ RH10 10K_0402_5% SD028100280
X76_M16G@ RH17 10K_0402_5% SD028100280	X76_M16G@ RH16 10K_0402_5% SD028100280	X76_M16G@ RH13 10K_0402_5% SD028100280	X76_M16G@ RH10 10K_0402_5% SD028100280
X76_M32G@ RH18 10K_0402_5% SD028100280	X76_M32G@ RH15 10K_0402_5% SD028100280	X76_M32G@ RH13 10K_0402_5% SD028100280	X76_M32G@ RH10 10K_0402_5% SD028100280
X76_H8G@ RH17 10K_0402_5% SD028100280	X76_H8G@ RH15 10K_0402_5% SD028100280	X76_H8G@ RH13 10K_0402_5% SD028100280	X76_H8G@ RH10 10K_0402_5% SD028100280
X76_H16G@ RH18 10K_0402_5% SD028100280	X76_H16G@ RH16 10K_0402_5% SD028100280	X76_H16G@ RH12 10K_0402_5% SD028100280	X76_H16G@ RH10 10K_0402_5% SD028100280
X76_H32G@ RH17 10K_0402_5% SD028100280	X76_H32G@ RH16 10K_0402_5% SD028100280	X76_H32G@ RH12 10K_0402_5% SD028100280	X76_H32G@ RH10 10K_0402_5% SD028100280
X76_S8G@ RH18 10K_0402_5% SD028100280	X76_S8G@ RH15 10K_0402_5% SD028100280	X76_S8G@ RH12 10K_0402_5% SD028100280	X76_S8G@ RH10 10K_0402_5% SD028100280
X76_S16G@ RH17 10K_0402_5% SD028100280	X76_S16G@ RH15 10K_0402_5% SD028100280	X76_S16G@ RH12 10K_0402_5% SD028100280	X76_S16G@ RH10 10K_0402_5% SD028100280
X76_S32G@ RH18 10K_0402_5% SD028100280	X76_S32G@ RH16 10K_0402_5% SD028100280	X76_S32G@ RH13 10K_0402_5% SD028100280	X76_S32G@ RH9 10K_0402_5% SD028100280

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Title: P05-MCP(1/14)DDI,EDP,CSI2,EMMC

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LPDDR3, Ballot for side by side(Non-Interleave)

19 DDR_A_DQS#[0..7]
19 DDR_A_DQS[0..7]
19 DDR_A_D[0..63]
19,21 DDR_A_CA1_[0..9]
19,21 DDR_A_CA2_[0..9]

20 DDR_B_DQS#[0..7]
20 DDR_B_DQS[0..7]
20 DDR_B_D[0..63]
20,21 DDR_B_CA1_[0..9]
20,21 DDR_B_CA2_[0..9]

@UCPU1B SKL-U

DDR_A_D0	AL71	DDR0_DQ[0]	AU53	DDR_A_CLK#0	DDR_A_CLK#0 19,21
DDR_A_D1	AL68	DDR0_DQ[1]	AT53	DDR_A_CLK0	DDR_A_CLK0 19,21
DDR_A_D2	AN68	DDR0_DQ[2]	AU55	DDR_A_CLK#1	DDR_A_CLK#1 19,21
DDR_A_D3	AN69	DDR0_DQ[3]	AT55	DDR_A_CLK1	DDR_A_CLK1 19,21
DDR_A_D4	AL70	DDR0_DQ[4]	BA56	DDR_A_CKE0	
DDR_A_D5	AL69	DDR0_DQ[5]	BB56	DDR_A_CKE1	DDR_A_CKE0 19,21
DDR_A_D6	AN70	DDR0_DQ[6]	AW56	DDR_A_CKE2	DDR_A_CKE1 19,21
DDR_A_D7	AN71	DDR0_DQ[7]	AY56	DDR_A_CKE3	DDR_A_CKE2 19,21
DDR_A_D8	AR70	DDR0_DQ[8]			DDR_A_CKE3 19,21
DDR_A_D9	AR68	DDR0_DQ[9]	AU45	DDR_A_CS#0	
DDR_A_D10	AU71	DDR0_DQ[10]	AU43	DDR_A_CS#1	DDR_A_CS#0 19,21
DDR_A_D11	AU68	DDR0_DQ[11]	AT45	DDR_A_ODT0	DDR_A_CS#1 19,21
DDR_A_D12	AR71	DDR0_DQ[12]	AT43		DDR_A_ODT0 19,21
DDR_A_D13	AR69	DDR0_DQ[13]			
DDR_A_D14	AU70	DDR0_DQ[14]	BA51		
DDR_A_D15	AU69	DDR0_DQ[15]	BB54		DDR_A_CA1_0 19,21
DDR_A_D32	BB65	DDR0_DQ[16]/DDR0_DQ[32]	BA52		DDR_A_CA1_1 19,21
DDR_A_D33	AW65	DDR0_DQ[17]/DDR0_DQ[33]	AY52		DDR_A_CA1_2 19,21
DDR_A_D34	AW63	DDR0_DQ[18]/DDR0_DQ[34]	AW52		DDR_A_CA1_3 19,21
DDR_A_D35	AY63	DDR0_DQ[19]/DDR0_DQ[35]	AY55		DDR_A_CA1_4 19,21
DDR_A_D36	BA65	DDR0_DQ[20]/DDR0_DQ[36]	AW54		DDR_A_CA1_5 19,21
DDR_A_D37	AY65	DDR0_DQ[21]/DDR0_DQ[37]	BA54		DDR_A_CA1_6 19,21
DDR_A_D38	BA63	DDR0_DQ[22]/DDR0_DQ[38]	BA55		DDR_A_CA1_7 19,21
DDR_A_D39	BB63	DDR0_DQ[23]/DDR0_DQ[39]	AY54		DDR_A_CA1_8 19,21
DDR_A_D40	BA61	DDR0_DQ[24]/DDR0_DQ[40]			DDR_A_CA1_9 19,21
DDR_A_D41	AW61	DDR0_DQ[25]/DDR0_DQ[41]	AU46		
DDR_A_D42	BB59	DDR0_DQ[26]/DDR0_DQ[42]	AU48		DDR_A_CA2_0 19,21
DDR_A_D43	AW59	DDR0_DQ[27]/DDR0_DQ[43]	AT46		DDR_A_CA2_1 19,21
DDR_A_D44	BB61	DDR0_DQ[28]/DDR0_DQ[44]	AU50		DDR_A_CA2_2 19,21
DDR_A_D45	AY61	DDR0_DQ[29]/DDR0_DQ[45]	AU52		DDR_A_CA2_3 19,21
DDR_A_D46	BA59	DDR0_DQ[30]/DDR0_DQ[46]	AY51		DDR_A_CA2_4 19,21
DDR_A_D47	AY59	DDR0_DQ[31]/DDR0_DQ[47]	AT48		DDR_A_CA2_5 19,21
DDR_B_D0	AY39	DDR0_DQ[32]/DDR1_DQ[0]	AT50		DDR_A_CA2_6 19,21
DDR_B_D1	AW39	DDR0_DQ[33]/DDR1_DQ[1]	BB50		DDR_A_CA2_7 19,21
DDR_B_D2	AY37	DDR0_DQ[34]/DDR1_DQ[2]	AY50		DDR_A_CA2_8 19,21
DDR_B_D3	AW37	DDR0_DQ[35]/DDR1_DQ[3]	BA50		DDR_A_CA2_9 19,21
DDR_B_D4	BB39	DDR0_DQ[36]/DDR1_DQ[4]	BB52		
DDR_B_D5	BA39	DDR0_DQ[37]/DDR1_DQ[5]			
DDR_B_D6	BA37	DDR0_DQ[38]/DDR1_DQ[6]	AM70		
DDR_B_D7	BB37	DDR0_DQ[39]/DDR1_DQ[7]	AM69		DDR_A_DQS#0 19
DDR_B_D8	AY35	DDR0_DQ[40]/DDR1_DQ[8]	AT69		DDR_A_DQS0 19
DDR_B_D9	AW35	DDR0_DQ[41]/DDR1_DQ[9]	AT70		DDR_A_DQS#1 19
DDR_B_D10	AY33	DDR0_DQ[42]/DDR1_DQ[10]	BA64		DDR_A_DQS1 19
DDR_B_D11	AW33	DDR0_DQ[43]/DDR1_DQ[11]	AY64		DDR_A_DQS#4 19
DDR_B_D12	BB35	DDR0_DQ[44]/DDR1_DQ[12]	AY60		DDR_A_DQS4 19
DDR_B_D13	BA35	DDR0_DQ[45]/DDR1_DQ[13]	BA60		DDR_A_DQS#5 19
DDR_B_D14	BA33	DDR0_DQ[46]/DDR1_DQ[14]	BA38		DDR_A_DQS5 19
DDR_B_D15	BB33	DDR0_DQ[47]/DDR1_DQ[15]	AY38		DDR_B_DQS#0 20
DDR_B_D32	AY31	DDR0_DQ[48]/DDR1_DQ[32]	AY34		DDR_B_DQS0 20
DDR_B_D33	AW31	DDR0_DQ[49]/DDR1_DQ[33]	BA34		DDR_B_DQS#1 20
DDR_B_D34	AY29	DDR0_DQ[50]/DDR1_DQ[34]	BA30		DDR_B_DQS1 20
DDR_B_D35	AW29	DDR0_DQ[51]/DDR1_DQ[35]	AY30		DDR_B_DQS#4 20
DDR_B_D36	BB31	DDR0_DQ[52]/DDR1_DQ[36]	AY26		DDR_B_DQS4 20
DDR_B_D37	BA31	DDR0_DQ[53]/DDR1_DQ[37]	BA26		DDR_B_DQS#5 20
DDR_B_D38	BA29	DDR0_DQ[54]/DDR1_DQ[38]			DDR_B_DQS5 20
DDR_B_D39	BB29	DDR0_DQ[55]/DDR1_DQ[39]	AW50		
DDR_B_D40	AY27	DDR0_DQ[56]/DDR1_DQ[40]	AT52		DDR0_ALERT#
DDR_B_D41	AW27	DDR0_DQ[57]/DDR1_DQ[41]			DDR0_PAR
DDR_B_D42	AY25	DDR0_DQ[58]/DDR1_DQ[42]	AY67		DDR_VREF_CA +V_DDR_REF_CA 21
DDR_B_D43	AW25	DDR0_DQ[59]/DDR1_DQ[43]	AY68		DDR0_VREF_DQ +V_DDR_REFA_R 21
DDR_B_D44	BB27	DDR0_DQ[60]/DDR1_DQ[44]	BA67		DDR1_VREF_DQ +V_DDR_REFB_R 21
DDR_B_D45	BA27	DDR0_DQ[61]/DDR1_DQ[45]			
DDR_B_D46	BA25	DDR0_DQ[62]/DDR1_DQ[46]	AW67	DDR_VTT_CNTL	DDR_VTT_CNTL
DDR_B_D47	BB25	DDR0_DQ[63]/DDR1_DQ[47]			

DDR CH - A

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@UCPU1C SKL-U

DDR_A_D16	AF65	DDR1_DQ[0]/DDR0_DQ[16]	AN45	DDR_B_CLK#0	
DDR_A_D17	AF64	DDR1_DQ[1]/DDR0_DQ[17]	AN46	DDR_B_CLK#1	DDR_B_CLK#0 20,21
DDR_A_D18	AK65	DDR1_DQ[2]/DDR0_DQ[18]	AP45	DDR_B_CLK0	DDR_B_CLK#1 20,21
DDR_A_D19	AK64	DDR1_DQ[3]/DDR0_DQ[19]	AP46	DDR_B_CLK1	DDR_B_CLK0 20,21
DDR_A_D20	AF66	DDR1_DQ[4]/DDR0_DQ[20]			DDR_B_CLK1 20,21
DDR_A_D21	AF67	DDR1_DQ[5]/DDR0_DQ[21]	AN56	DDR_B_CKE0	
DDR_A_D22	AK67	DDR1_DQ[6]/DDR0_DQ[22]	AP55	DDR_B_CKE1	DDR_B_CKE0 20,21
DDR_A_D23	AK66	DDR1_DQ[7]/DDR0_DQ[23]	AN55	DDR_B_CKE2	DDR_B_CKE1 20,21
DDR_A_D24	AF70	DDR1_DQ[8]/DDR0_DQ[24]	AP53	DDR_B_CKE3	DDR_B_CKE2 20,21
DDR_A_D25	AF68	DDR1_DQ[9]/DDR0_DQ[25]			DDR_B_CKE3 20,21
DDR_A_D26	AH71	DDR1_DQ[10]/DDR0_DQ[26]	BB42	DDR_B_CS#0	
DDR_A_D27	AH68	DDR1_DQ[11]/DDR0_DQ[27]	AY42	DDR_B_CS#1	DDR_B_CS#0 20,21
DDR_A_D28	AF71	DDR1_DQ[12]/DDR0_DQ[28]	BA42	DDR_B_ODT0	DDR_B_CS#1 20,21
DDR_A_D29	AF69	DDR1_DQ[13]/DDR0_DQ[29]	AW42		DDR_B_ODT0 20,21
DDR_A_D30	AH70	DDR1_DQ[14]/DDR0_DQ[30]			
DDR_A_D31	AH69	DDR1_DQ[15]/DDR0_DQ[31]	AY48		
DDR_A_D48	AT66	DDR1_DQ[16]/DDR0_DQ[48]	AP50		DDR_B_CA1_0 20,21
DDR_A_D49	AU66	DDR1_DQ[17]/DDR0_DQ[49]	BA48		DDR_B_CA1_1 20,21
DDR_A_D50	AP65	DDR1_DQ[18]/DDR0_DQ[50]	BB48		DDR_B_CA1_2 20,21
DDR_A_D51	AN65	DDR1_DQ[19]/DDR0_DQ[51]	AP48		DDR_B_CA1_3 20,21
DDR_A_D52	AN66	DDR1_DQ[20]/DDR0_DQ[52]	AP52		DDR_B_CA1_4 20,21
DDR_A_D53	AP66	DDR1_DQ[21]/DDR0_DQ[53]	AN50		DDR_B_CA1_5 20,21
DDR_A_D54	AT65	DDR1_DQ[22]/DDR0_DQ[54]	AN48		DDR_B_CA1_6 20,21
DDR_A_D55	AU65	DDR1_DQ[23]/DDR0_DQ[55]	AN53		DDR_B_CA1_7 20,21
DDR_A_D56	AT61	DDR1_DQ[24]/DDR0_DQ[56]	AN52		DDR_B_CA1_8 20,21
DDR_A_D57	AU61	DDR1_DQ[25]/DDR0_DQ[57]			DDR_B_CA1_9 20,21
DDR_A_D58	AP60	DDR1_DQ[26]/DDR0_DQ[58]	BA43		
DDR_A_D59	AN60	DDR1_DQ[27]/DDR0_DQ[59]	AY43		DDR_B_CA2_0 20,21
DDR_A_D60	AN61	DDR1_DQ[28]/DDR0_DQ[60]	AY44		DDR_B_CA2_1 20,21
DDR_A_D61	AP61	DDR1_DQ[29]/DDR0_DQ[61]	AW44		DDR_B_CA2_2 20,21
DDR_A_D62	AT60	DDR1_DQ[30]/DDR0_DQ[62]	BB44		DDR_B_CA2_3 20,21
DDR_A_D63	AU60	DDR1_DQ[31]/DDR0_DQ[63]	AY47		DDR_B_CA2_4 20,21
DDR_B_D16	AU40	DDR1_DQ[32]/DDR1_DQ[16]	BA44		DDR_B_CA2_5 20,21
DDR_B_D17	AT40	DDR1_DQ[33]/DDR1_DQ[17]	AW46		DDR_B_CA2_6 20,21
DDR_B_D18	AT37	DDR1_DQ[34]/DDR1_DQ[18]	AY46		DDR_B_CA2_7 20,21
DDR_B_D19	AU37	DDR1_DQ[35]/DDR1_DQ[19]	BA46		DDR_B_CA2_8 20,21
DDR_B_D20	AR40	DDR1_DQ[36]/DDR1_DQ[20]	BB46		DDR_B_CA2_9 20,21
DDR_B_D21	AP40	DDR1_DQ[37]/DDR1_DQ[21]	BA47		
DDR_B_D22	AP37	DDR1_DQ[38]/DDR1_DQ[22]			
DDR_B_D23	AR37	DDR1_DQ[39]/DDR1_DQ[23]	AH66		
DDR_B_D24	AT33	DDR1_DQ[40]/DDR1_DQ[24]	AH65		DDR_A_DQS#2 19
DDR_B_D25	AU33	DDR1_DQ[41]/DDR1_DQ[25]	AG69		DDR_A_DQS2 19
DDR_B_D26	AU30	DDR1_DQ[42]/DDR1_DQ[26]	AG70		DDR_A_DQS#3 19
DDR_B_D27	AT30	DDR1_DQ[43]/DDR1_DQ[27]	AR66		DDR_A_DQS3 19
DDR_B_D28	AR33	DDR1_DQ[44]/DDR1_DQ[28]	AR65		DDR_A_DQS#6 19
DDR_B_D29	AP33	DDR1_DQ[45]/DDR1_DQ[29]	AR61		DDR_A_DQS6 19
DDR_B_D30	AR30	DDR1_DQ[46]/DDR1_DQ[30]	AR60		DDR_A_DQS#7 19
DDR_B_D31	AP30	DDR1_DQ[47]/DDR1_DQ[31]	AT38		DDR_A_DQS7 19
DDR_B_D48	AU27	DDR1_DQ[48]	AR38		DDR_B_DQS#2 20
DDR_B_D49	AT27	DDR1_DQ[49]	AT32		DDR_B_DQS2 20
DDR_B_D50	AT25	DDR1_DQ[50]	AR32		DDR_B_DQS#3 20
DDR_B_D51	AU25	DDR1_DQ[51]	AR25		DDR_B_DQS3 20
DDR_B_D52	AP27	DDR1_DQ[52]	AR27		DDR_B_DQS#6 20
DDR_B_D53	AN27	DDR1_DQ[53]	AR22		DDR_B_DQS6 20
DDR_B_D54	AN25	DDR1_DQ[54]	AR21		DDR_B_DQS#7 20
DDR_B_D55	AP25	DDR1_DQ[55]			DDR_B_DQS7 20
DDR_B_D56	AT22	DDR1_DQ[56]	AN43		
DDR_B_D57	AU22	DDR1_DQ[57]	AP43		DDR1_ALERT#
DDR_B_D58	AU21	DDR1_DQ[58]	AT13		DDR1_PAR
DDR_B_D59	AT21	DDR1_DQ[59]	AR18	SM_RCOMP0	DRAM_RESET#
DDR_B_D60	AN22	DDR1_DQ[60]	AT18	SM_RCOMP1	DDR_RCOMP[0]
DDR_B_D62	AP21	DDR1_DQ[61]	AU18	SM_RCOMP2	DDR_RCOMP[1]
DDR_B_D63	AN21	DDR1_DQ[62]			DDR_RCOMP[2]
		DDR1_DQ[63]			

PAD~D @T36

DDR CH - B

SKL-U_BGA1356 3 OF 20

+1.2V_DDR

UC1
74AUP1G07GW_TSSOP5
1 NC
2 A
3 GND
5 VCC
4 Y

DDR_VTT_CNTL

CC15
0.1U_0402_10V7K

+3VS

R32
100K_0402_5%

SM_PG_CTRL 53

Use SA00005U600

LPDDR3 COMPENSATION SIGNALS

SM_RCOMP0 RC164 1 2 200_0402_1%
SM_RCOMP1 RC166 1 2 80.6_0402_1%
SM_RCOMP2 RC165 1 2 162_0402_1%

CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P06-MCP(2/14)LPDDR3

Size: | Document Number: LA-F371P | Rev: 1.0

Date: Tuesday, November 07, 2017 | Sheet 6 of 65

PVT-023
Change 0 ohm to short pad

+1.8VA — R513 — +1.8V_ESPI
0_0201_5%

SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

PVT-048
De-pop debug XDP related components

13 PCH_SPI_DO_XDP — @XDP@ RC60 1K_0402_5%
13 PCH_SPI_DO2_XDP — @XDP@ RC61 1K_0402_5%

@UCPU1E — SKL-U

SPI - FLASH
PCH_SPI_CLK AV2 — SPI0_CLK
PCH_SPI_SO AW3 — SPI0_MISO
PCH_SPI_SI AV3 — SPI0_MOSI
PCH_SPI_IO2 AW2 — SPI0_IO2
PCH_SPI_IO3 AU4 — SPI0_IO3
PCH_SPI_CS0# AU3 — SPI0_CS0#
PCH_SPI_CS1# AU2 — SPI0_CS1#
31 PCH_SPI_CS2# — AU1 — SPI0_CS2#

SPI - TOUCH
M2 — GPP_D1/SPI1_CLK
M3 — GPP_D2/SPI1_MISO
J4 — GPP_D3/SPI1_MOSI
V1 — GPP_D21/SPI1_IO2
V2 — GPP_D22/SPI1_IO3
M1 — GPP_D0/SPI1_CS#

C LINK
24 CL_CLK — G3 — CL_CLK
24 CL_DATA — G2 — CL_DATA
24 CL_RST# — G1 — CL_RST#

SMBUS, SMLINK
GPP_C0/SMBCLK — R7 — DDR_XDP_SMBCLK — DDR_XDP_SMBCLK 13
GPP_C1/SMBDATA — R8 — DDR_XDP_SMBDAT — DDR_XDP_SMBDAT 13
GPP_C2/SMBALERT# — R10 — PCH_SMB_ALERT#
GPP_C3/SML0CLK — R9
GPP_C4/SML0DATA — V2
GPP_C5/SML0ALERT# — W1 — GPP_C5
GPP_C6/SML1CLK — W3 — SML1_SMBCLK — SML1_SMBCLK 30
GPP_C7/SML1DATA — V3 — SML1_SMBDAT — SML1_SMBDAT 30
GPP_B23/SML1ALERT#/PCHHOT# — AM7 — GPP_B23

LPC
GPP_A1/LAD0/ESPI_IO0 — AY13 — ESPI_IO0_R — RC3831 2 15_0402_5% — ESPI_IO0 30,43
GPP_A2/LAD1/ESPI_IO1 — BA13 — ESPI_IO1_R — RC3841 2 15_0402_5% — ESPI_IO1 30,43
GPP_A3/LAD2/ESPI_IO2 — BB13 — ESPI_IO2_R — RC3851 2 15_0402_5% — ESPI_IO2 30,43
GPP_A4/LAD3/ESPI_IO3 — AY12 — ESPI_IO3_R — RC3861 2 15_0402_5% — ESPI_IO3 30,43
GPP_A5/LFRAME#/ESPI_CS# — BA12 — ESPI_CS# 30,43
GPP_A14/SUS_STAT#/ESPI_RESET# — BA11 — ESPI_RESET# 30
RFQ-034
change LPC to ESPI mode

GPP_A9/CLKOUT_LPC0/ESPI_CLK — AW9 — PCI_CLK_LPC0
GPP_A10/CLKOUT_LPC1 — AY9 — PCI_CLK_LPC1 — @RC70 1 — RC71 1 2 15_0402_5% — ESPI_CLK 30,43
GPP_A8/CLKRUN# — AW11 — CLKRUN#

SKL-U_BGA1356

ESPI_CLK — 12P_0402_50V8J — EMC@ CC78
Reserve for RF

+1.8V_ESPI — RC83 1 — 2 10K_0402_5% — ESPI_ALERT#
8,31 TPM_PIRQ# — @RC1981 — TC1 2 0_0201_5%

+1.8V_PGPP — @RC73 1 — 2 10K_0402_5% — SIO_RCIN#
SIO_RCIN# — AW13 — GPP_A0/RCIN#
30 ESPI_ALERT# — ESPI_ALERT# — AY11 — GPP_A6/SERIRQ

+3VS
DDR_XDP_SMBDAT — 2.2K_0402_5% — RN1
DDR_XDP_SMBCLK — 2.2K_0402_5% — RN2
CLKRUN# — 8.2K_0402_5% — @RC82

+3V_PRIM
SML1_SMBCLK — RC55 1K_0402_5%
SML1_SMBDAT — RC51 1K_0402_5%

5 OF 20
RP2
SPI_SI_VROM1 — PCH_SPI_SI
SPI_CLK_VROM1 — PCH_SPI_CLK
31 PCH_SPI_CLK_TPM
31 PCH_SPI_SI_TPM
33_0804_8P4R_5%

RP3
31 PCH_SPI_SO_TPM
SPI_SO_VROM1 — PCH_SPI_SO
SPI_IO2_VROM1 — PCH_SPI_IO2
SPI_IO3_VROM1 — PCH_SPI_IO3
33_0804_8P4R_5%

SPI_CLK_VROM1 — 33_0402_5% @RC169 — 33P_0402_50V8J @CC91

+3.3V_SPI — CC90 0.1U_0402_25V6

128Mb Flash ROM
UH1
PCH_SPI_CS0# — CS# — VCC — SPI_IO3_VROM1
SPI_SO_VROM1 — DO — HOLD#_RESET# — SPI_CLK_VROM1
SPI_IO2_VROM1 — WP# — CLK — SPI_SI_VROM1
GND — DI
ThemalPad
W25Q128JVEIQ_WSON8_8X6

change RC49 to 2.2k
+3V_PRIM — PCH_SMB_ALERT# — RC49 2.2K_0402_5%

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

+3V_PRIM — GPP_C5 — RC58 4.7K_0201_5%

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

+3V_PRIM — GPP_B23 — @RC64 150K_0201_1%

EXI BOOT STALL BYPASS

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

SPI debug conn

JSPI2
PCH_SPI_CS1# 1
PCH_SPI_SI 2
PCH_SPI_SO 3
PCH_SPI_CLK 4
PCH_SPI_CS0# 5
PCH_SPI_IO2 6
PCH_SPI_IO3 7
+3.3V_SPI 8
+3V_PRIM 9
10
11 GND1
12 GND2
ACES_50521-01041-P01
CONN@

PCH — SPI
TPM
JSPI

+3V_PRIM
@RH19 1 — 2 1K_0402_5%~D — PCH_SPI_IO2
@RH20 1 — 2 1K_0402_5%~D — PCH_SPI_IO3
@RH21 1 — 2 1K_0402_5%~D — PCH_SPI_IO3

9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the
required 1 kOhm pull-up resistor(MOW WW5).
In this case, customers must ensure that the SPI
flash device on the platform has HOLD function ality disabled by default.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms
with ES and SKL S/H platforms with pre-ES1/ES1 samples(MOW WW9).

PVT-023
Change 0 ohm to short pad
+3V_PRIM — RC170 — +3.3V_SPI
0_0402_1%

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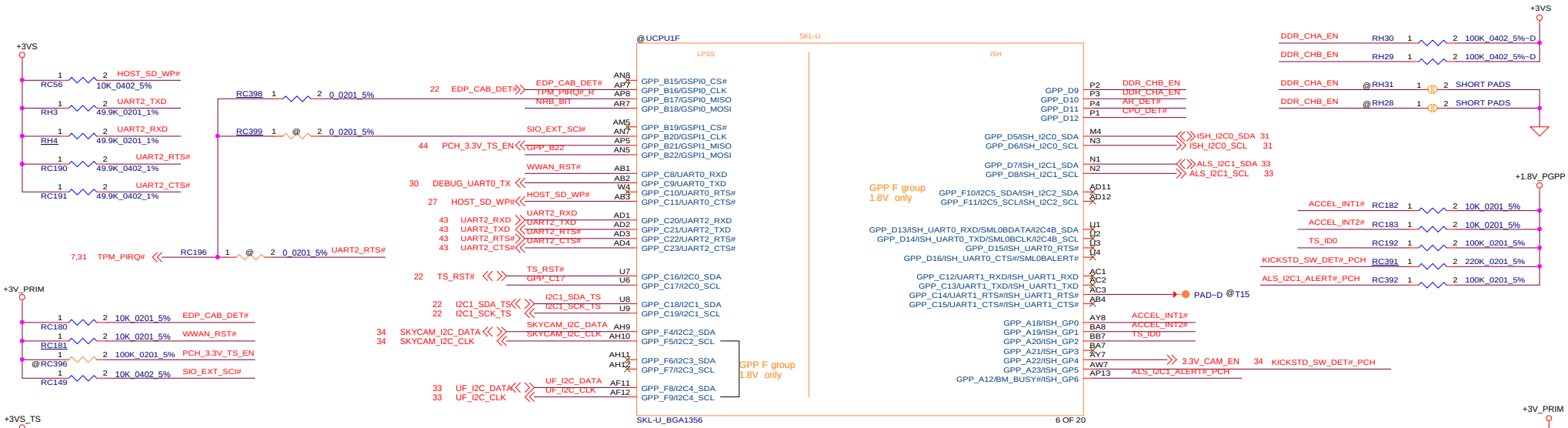
Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P07-MCP(3/14)SPI,SMB,LPC

Size	Document Number	Rev
	LA-F371P	1.0

Date: Tuesday, November 07, 2017 — Sheet 7 of 65



X76 DRAM Option (R3)

X7669231L56	**Micron 8G/1866** MICRON_8G_R3@ UD1 MT52L256M32D1PF-107WT SA00009XU1L MICRON_8G_R3@ UD2 MT52L256M32D1PF-107WT SA00009XU1L MICRON_8G_R3@ UD3 MT52L256M32D1PF-107WT SA00009XU1L MICRON_8G_R3@ UD4 MT52L256M32D1PF-107WT SA00009XU1L
X7669231L52	**Micron 16G/1866** MICRON_16G_R3@ UD1 MT52L512M32D2PF-107WT SA00009U71L MICRON_16G_R3@ UD2 MT52L512M32D2PF-107WT SA00009U71L MICRON_16G_R3@ UD3 MT52L512M32D2PF-107WT SA00009U71L MICRON_16G_R3@ UD4 MT52L512M32D2PF-107WT SA00009U71L
X7669231L54	**Micron 32G/1866** MICRON_32G_R3@ UD1 MT52L1G32D4PG-107WT SA00009XY1L MICRON_32G_R3@ UD2 MT52L1G32D4PG-107WT SA00009XY1L MICRON_32G_R3@ UD3 MT52L1G32D4PG-107WT SA00009XY1L MICRON_32G_R3@ UD4 MT52L1G32D4PG-107WT SA00009XY1L
X7669231L51	**Hynix 8G/1866** HYNIX_8G_R3@ UD1 H9CCNNN8GTMLAR-NUD FBGA SA00008G65L HYNIX_8G_R3@ UD2 H9CCNNN8GTMLAR-NUD FBGA SA00008G65L HYNIX_8G_R3@ UD3 H9CCNNN8GTMLAR-NUD FBGA SA00008G65L HYNIX_8G_R3@ UD4 H9CCNNN8GTMLAR-NUD FBGA SA00008G65L
X7669231L53	**Hynix 16G/1866** HYNIX_16G_R3@ UD1 H9CCNNNBJTMLAR-NUD FBGA SA00008FJ5L HYNIX_16G_R3@ UD2 H9CCNNNBJTMLAR-NUD FBGA SA00008FJ5L HYNIX_16G_R3@ UD3 H9CCNNNBJTMLAR-NUD FBGA SA00008FJ5L HYNIX_16G_R3@ UD4 H9CCNNNBJTMLAR-NUD FBGA SA00008FJ5L
X7669231L55	**Hynix 32G/1866** HYNIX_32G_R3@ UD1 H9CCNNNCLTMLAR-NUD FBGA SA0000AEN1L HYNIX_32G_R3@ UD2 H9CCNNNCLTMLAR-NUD FBGA SA0000AEN1L HYNIX_32G_R3@ UD3 H9CCNNNCLTMLAR-NUD FBGA SA0000AEN1L HYNIX_32G_R3@ UD4 H9CCNNNCLTMLAR-NUD FBGA SA0000AEN1L
X7669231L57	X76_8G_R3@ X768G3 X76 X7669231L57 **Samsung 8G/1866** SAMSUNG_8G_R3@ UD1 K4E8E324EB-EGCF FBGA178P SA00009XY1L SAMSUNG_8G_R3@ UD2 K4E8E324EB-EGCF FBGA178P SA00009XY1L SAMSUNG_8G_R3@ UD3 K4E8E324EB-EGCF FBGA178P SA00009XY1L SAMSUNG_8G_R3@ UD4 K4E8E324EB-EGCF FBGA178P SA00009XY1L
X7669231L58	X76_16G_R3@ X7616G3 X76 X7669231L58 **Samsung 16G/1866** SAMSUNG_16G_R3@ UD1 K4E6E304EB-EGCF FBGA17 SA00008QV3L SAMSUNG_16G_R3@ UD2 K4E6E304EB-EGCF FBGA17 SA00008QV3L SAMSUNG_16G_R3@ UD3 K4E6E304EB-EGCF FBGA17 SA00008QV3L SAMSUNG_16G_R3@ UD4 K4E6E304EB-EGCF FBGA17 SA00008QV3L
X7669231L59	X76_32G_R3@ X7632G3 X76 X7669231L59 **Samsung 32G/1866** SAMSUNG_32G_R3@ UD1 4EBE304EB-EGCF FBGA178 SA00008X11L SAMSUNG_32G_R3@ UD2 4EBE304EB-EGCF FBGA178 SA00008X11L SAMSUNG_32G_R3@ UD3 4EBE304EB-EGCF FBGA178 SA00008X11L SAMSUNG_32G_R3@ UD4 4EBE304EB-EGCF FBGA178 SA00008X11L

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

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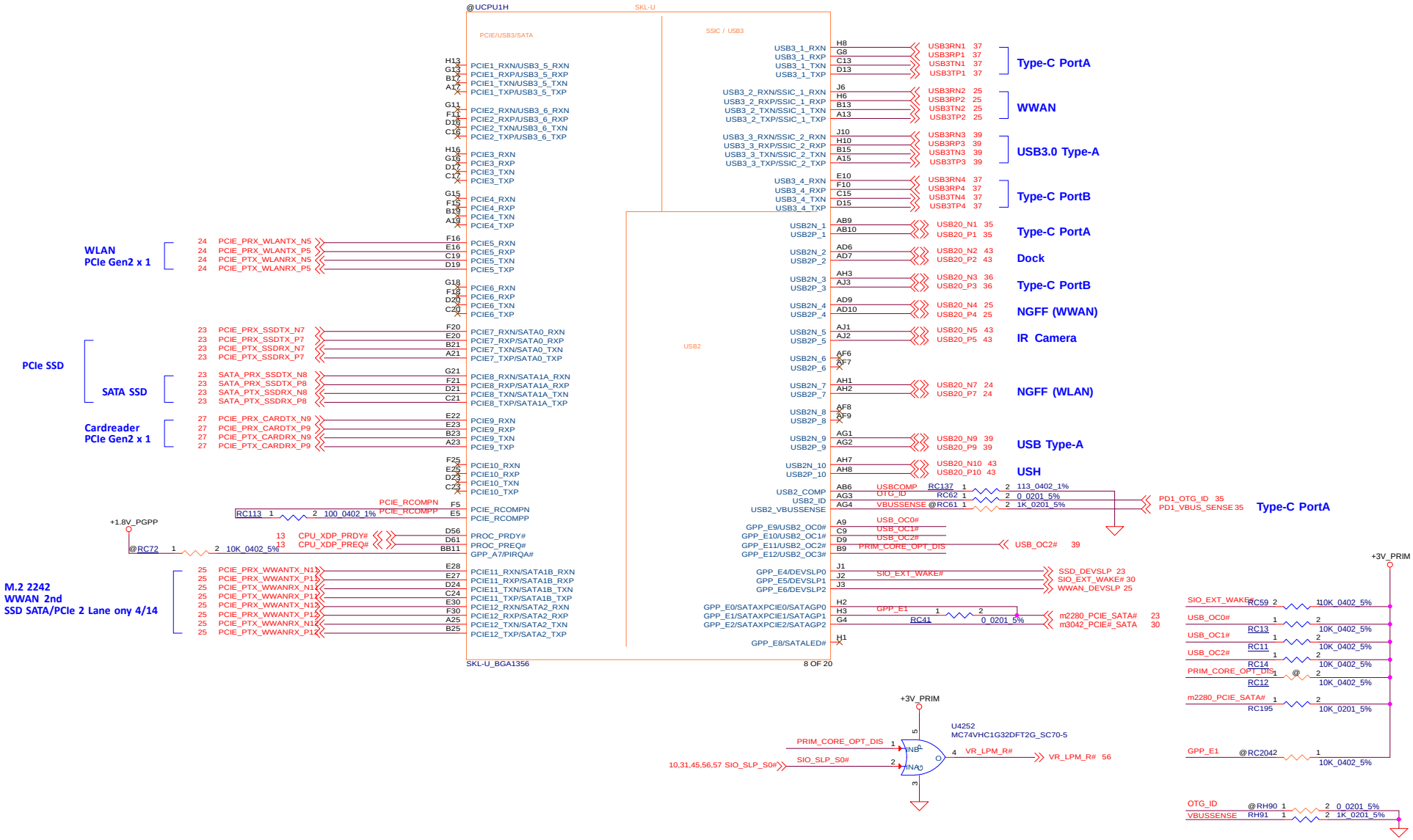
Compal Electronics, Inc.

Title: *P08-MCP(4/14)GSPI,I2C,UART,ISH*

Size	Document Number	Rev
	LA-F371P	1.0

Date: Tuesday, November 07, 2017 Sheet 8 of 65



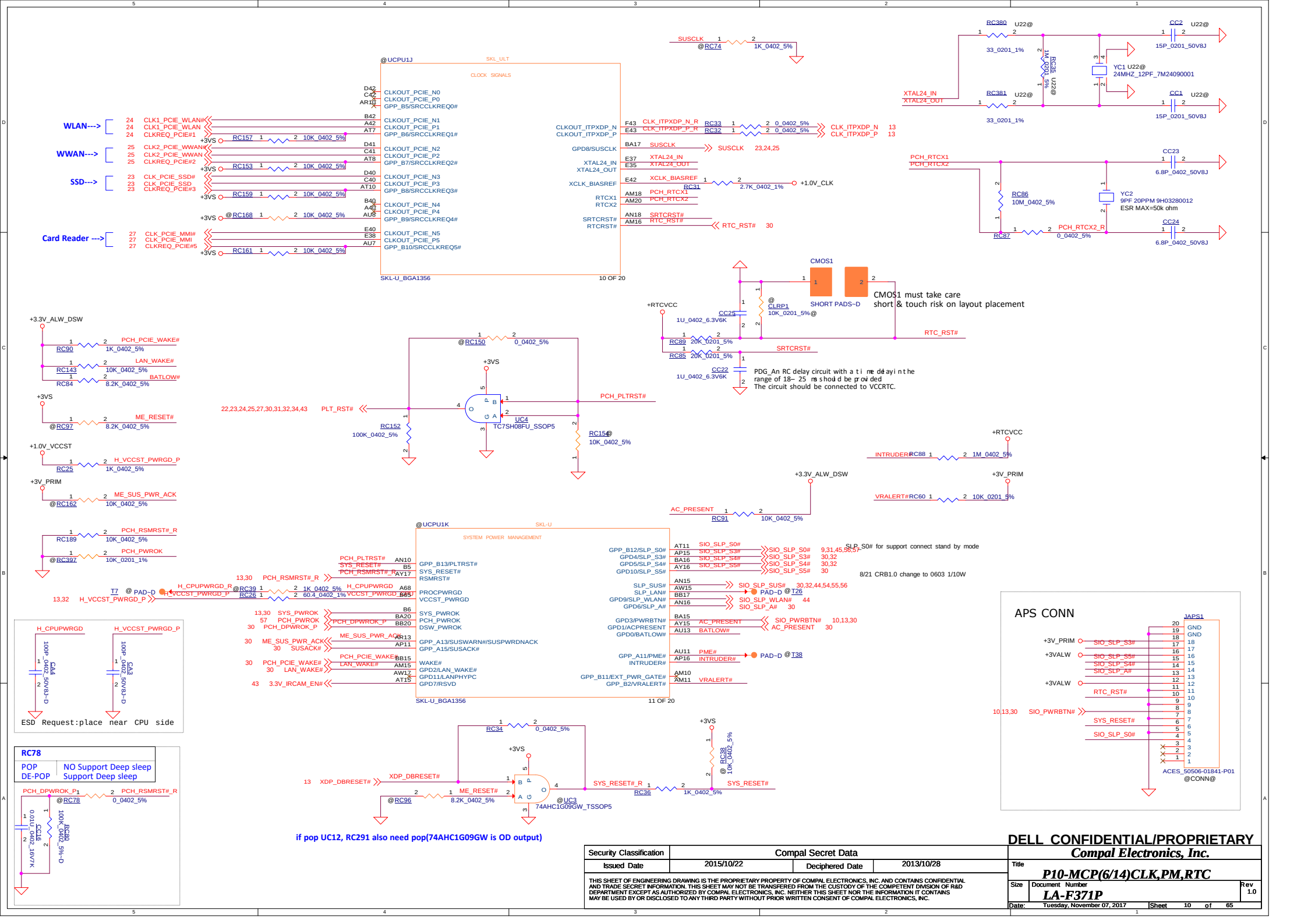
Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P09-MCP(5/14)PCIE,USB,SATA*

Size	Document Number	Rev
	LA-F371P	1.0

Date: Tuesday, November 07, 2017 Sheet 9 of 65

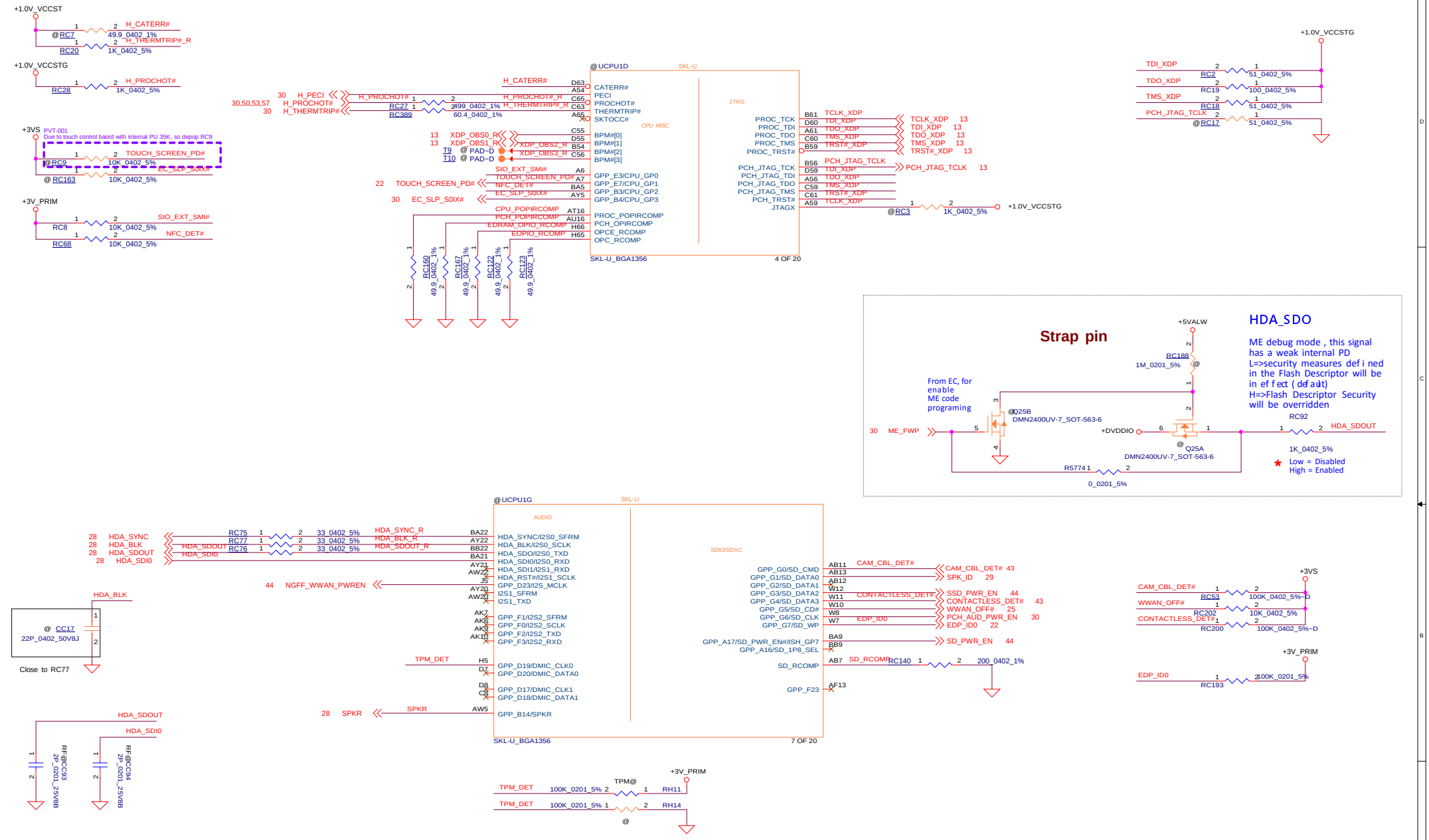


Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title	*P10-MCP(6/14)CLK,PM,RTC*	
Size	Document Number *LA-F371P*	Rev 1.0
Date: Tuesday, November 07, 2017	Sheet 10 of 65	



Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

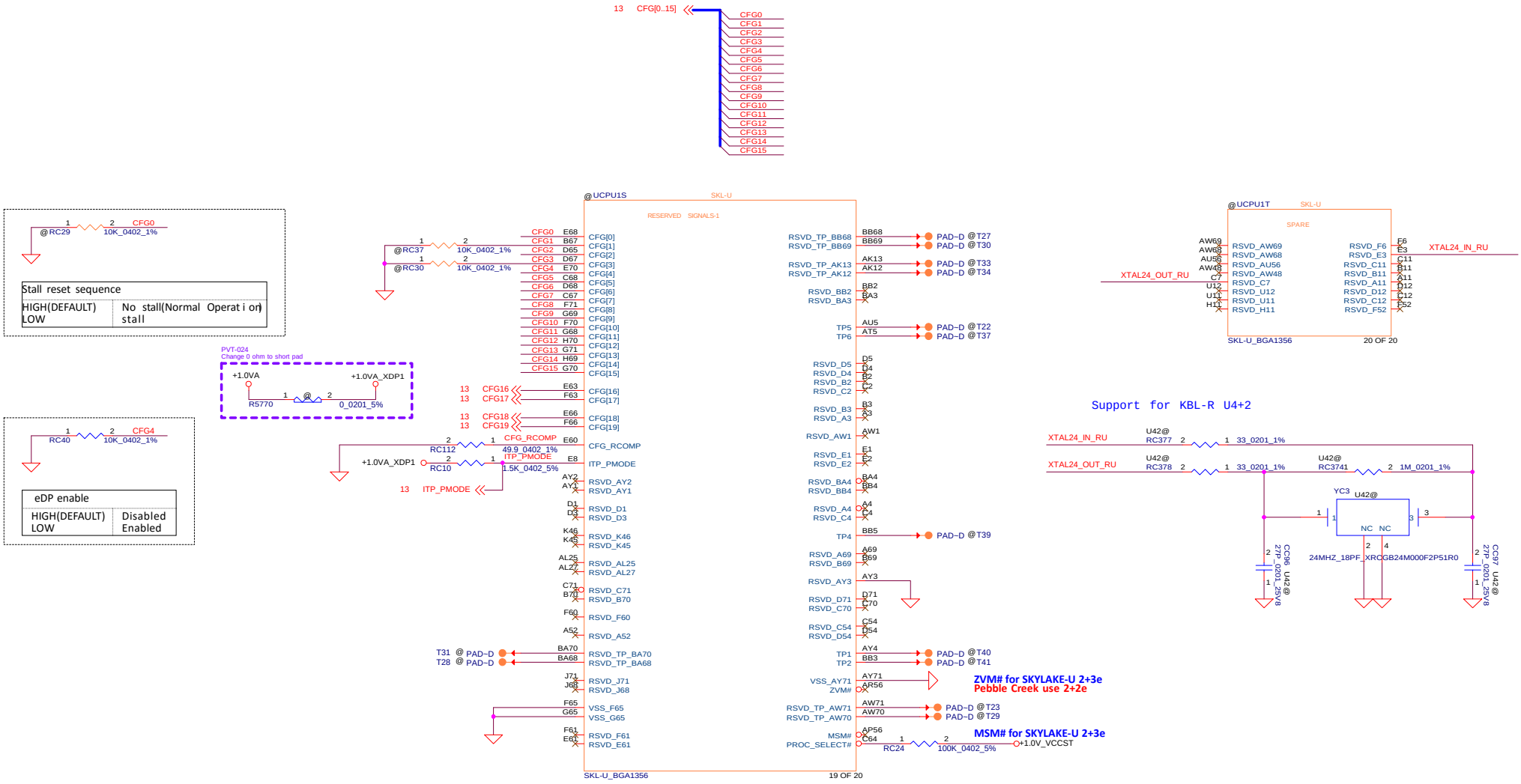
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: *P11-MCP(7/14)MISC,JTAG,HDA,SDIO*

Size: Document Number: *LA-F371P* Rev: 1.0

Date: Tuesday, November 07, 2017 Sheet 11 of 65



X76	32Gb 2133 DRAM Option (R1) , (R3)	DRAM Config Option (Resistor pop location) MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3
X7669231L60	**Micron 32G/2133** Micron 32G_R3@ UD1 MT52L1G32D4PG-107WT SA00009ZN1L	Micron 32G_R3@ UD2 MT52L1G32D4PG-107WT SA00009ZN1L	Micron 32G_R3@ UD3 MT52L1G32D4PG-107WT SA00009ZN1L	Micron 32G_R3@ UD4 MT52L1G32D4PG-107WT SA00009ZN1L	X76_M32G@ RH17 10K_0402_5% SD028100280	X76_M32G@ RH16 10K_0402_5% SD028100280	X76_M32G@ RH13 10K_0402_5% SD028100280	X76_M32G@ RH9 10K_0402_5% SD028100280
X7669231L62	**Hynix 32G/2133** HYNIX_32G_@ UD1 H9CCNNNCLGALAR-NVD FBGA SA00009ZL0L	HYNIX_32G_@ UD2 H9CCNNNCLGALAR-NVD FBGA SA00009ZL0L	HYNIX_32G_@ UD3 H9CCNNNCLGALAR-NVD FBGA SA00009ZL0L	HYNIX_32G_@ UD4 H9CCNNNCLGALAR-NVD FBGA SA00009ZL0L	X76_H32G@ RH18 10K_0402_5% SD028100280	X76_H32G@ RH15 10K_0402_5% SD028100280	X76_H32G@ RH13 10K_0402_5% SD028100280	X76_H32G@ RH9 10K_0402_5% SD028100280
X7669231L61	**Samsung 32G/2133** SAMSUNG_32G@ UD1 K4EBE304EB-EGCG FBGA178 SA00008VV0L	SAMSUNG_32G@ UD2 K4EBE304EB-EGCG FBGA178 SA00008VV0L	SAMSUNG_32G@ UD3 K4EBE304EB-EGCG FBGA178 SA00008VV0L	SAMSUNG_32G@ UD4 K4EBE304EB-EGCG FBGA178 SA00008VV0L	X76_S32G@ RH17 10K_0402_5% SD028100280	X76_S32G@ RH15 10K_0402_5% SD028100280	X76_S32G@ RH13 10K_0402_5% SD028100280	X76_S32G@ RH9 10K_0402_5% SD028100280

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: *P12-MCP(8/14)CFG,RSVD*

Size: Document Number: *LA-F371P* Rev: 1.0

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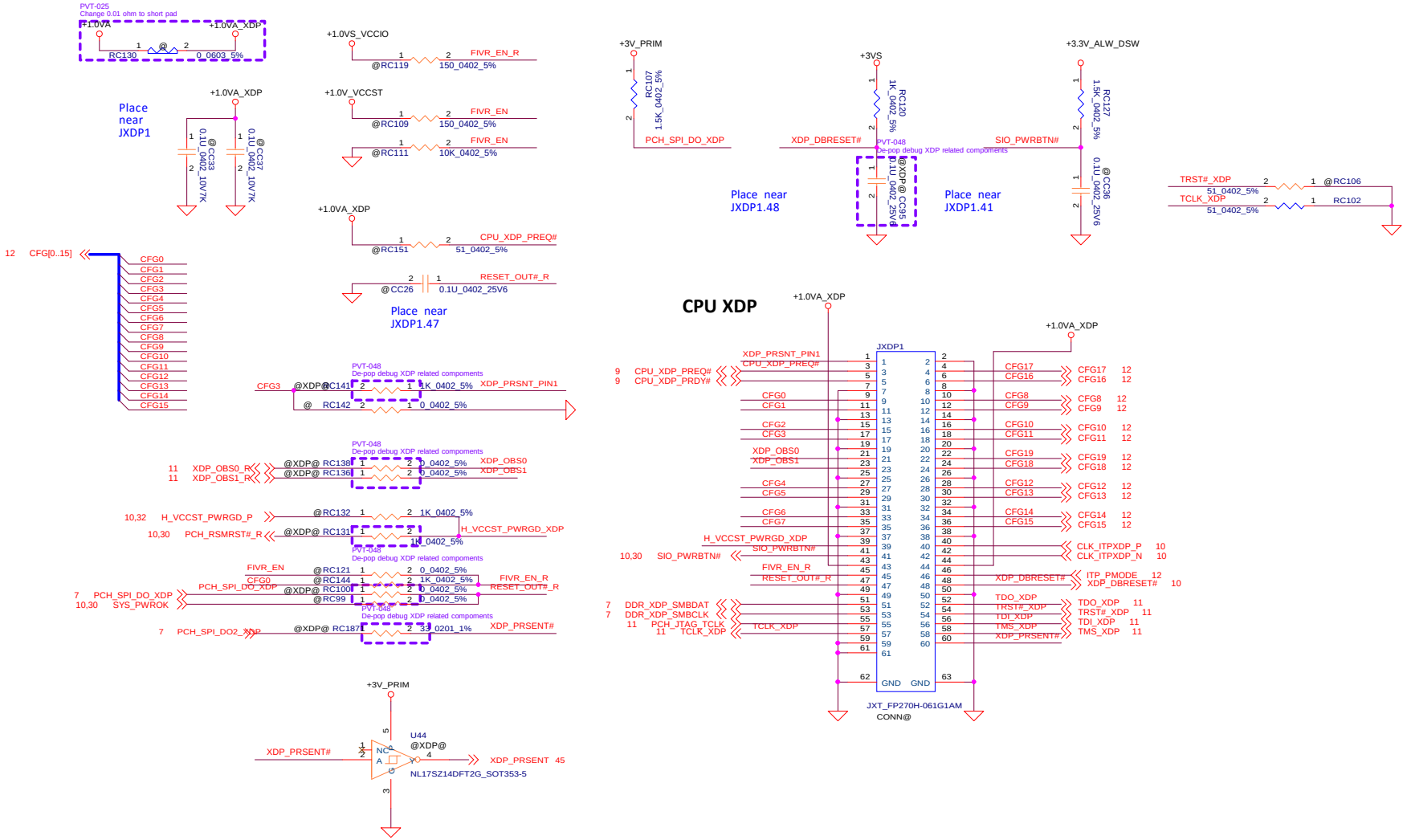

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Compal Electronics, Inc.

Title: P13-MCP(9/14)XDP

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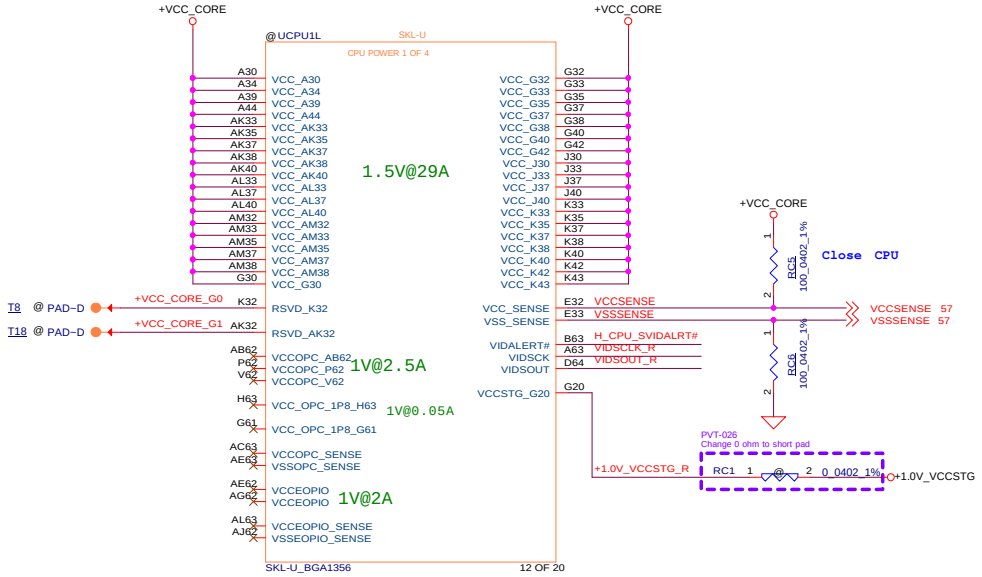
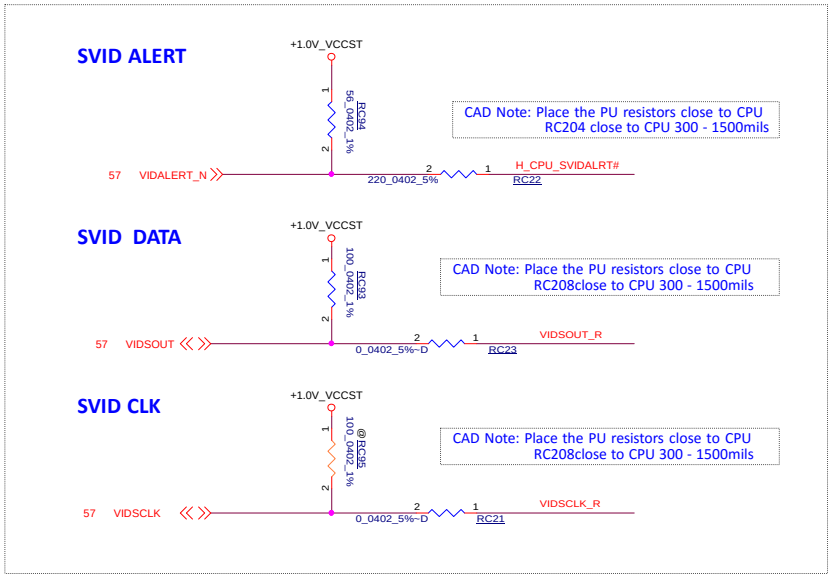
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A
+V1.8S_EDRAM: 1.8V, 50mA
+VCC_EOPIO: 0.8~1V, 2A



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



CDI#61280
10.2.7 SVID Topology
Table 10-9. SVID Bus Routing Guidelines
need double pull high

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: ***P14-MCP(10/14)PWR-VCC CORE***

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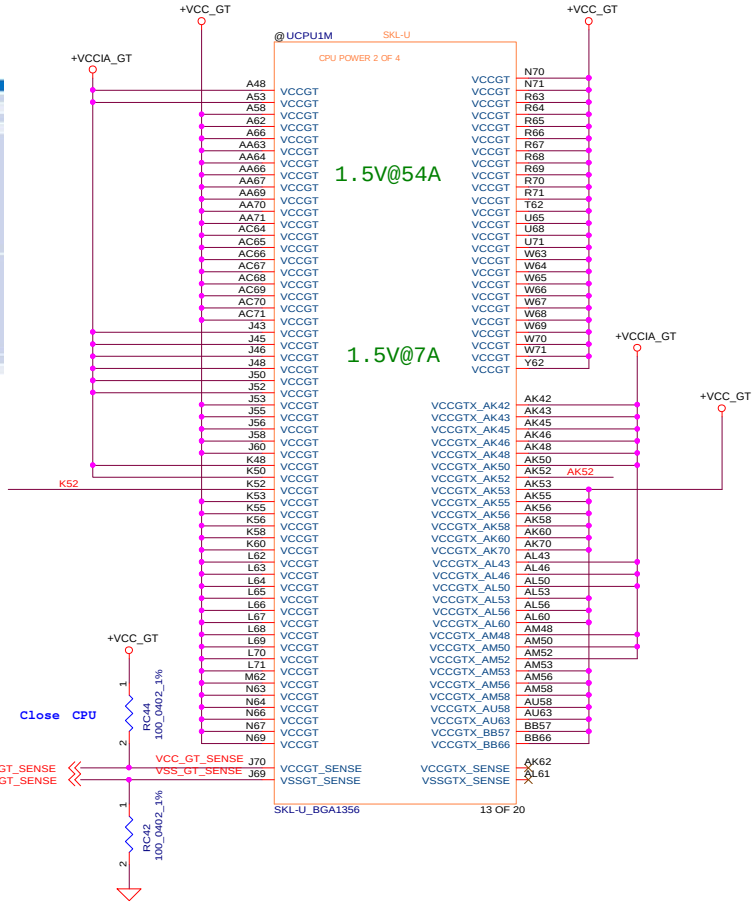
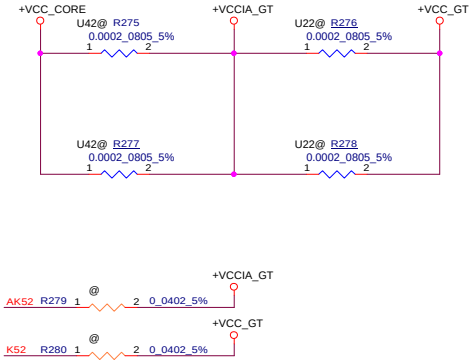
+VCCGT: 0.55~1.5V, 54A
+VCCGTX : 0.55~1.5V, 7A

Ball #	Ball Names R-U42	Ball Names U22	R-U42/U22 common board guidelines
C7	XTAL24_OUT	NC	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN	NC	connect to R-U42 XTAL24_IN
E39	NC	XTAL24_OUT	connect to U22 XTAL24_OUT
E37	NC	XTAL24_IN	connect to U22 XTAL24_IN
AK42	VCCCORE	VccGTx	
AK43	VCCCORE	VccGTx	
AK45	VCCCORE	VccGTx	
AK46	VCCCORE	VccGTx	
AK48	VCCCORE	VccGTx	
AK50	VCCCORE	VccGTx	connect to VccGTx/VCCCORE
AL42	VCCCORE	VccGTx	power plane island
AL46	VCCCORE	VccGTx	
AL50	VCCCORE	VccGTx	
AM48	VCCCORE	VccGTx	
AM50	VCCCORE	VccGTx	
AM52	VCCCORE	VccGTx	
J43	VCCCORE	VCCGT	
J45	VCCCORE	VCCGT	
J46	VCCCORE	VCCGT	
J48	VCCCORE	VCCGT	
J50	VCCCORE	VCCGT	connect to VccGTx/VCCCORE
J52	VCCCORE	VCCGT	power plane island
K48	VCCCORE	VCCGT	
K50	VCCCORE	VCCGT	
A48	VCCCORE	VCCGT	
AS3	VCCCORE	VCCGT	
AK52	RSVD	VccGTx	**Must Not Be Connected.** RVP use this signal for debug and testing purpose only.
K52	RSVD	VCCGT	**Must Not Be Connected.** RVP use this signal for debug and testing purpose only.





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Compal Electronics, Inc.

Title: P15-MCP(11/14)PWR-VCCGT

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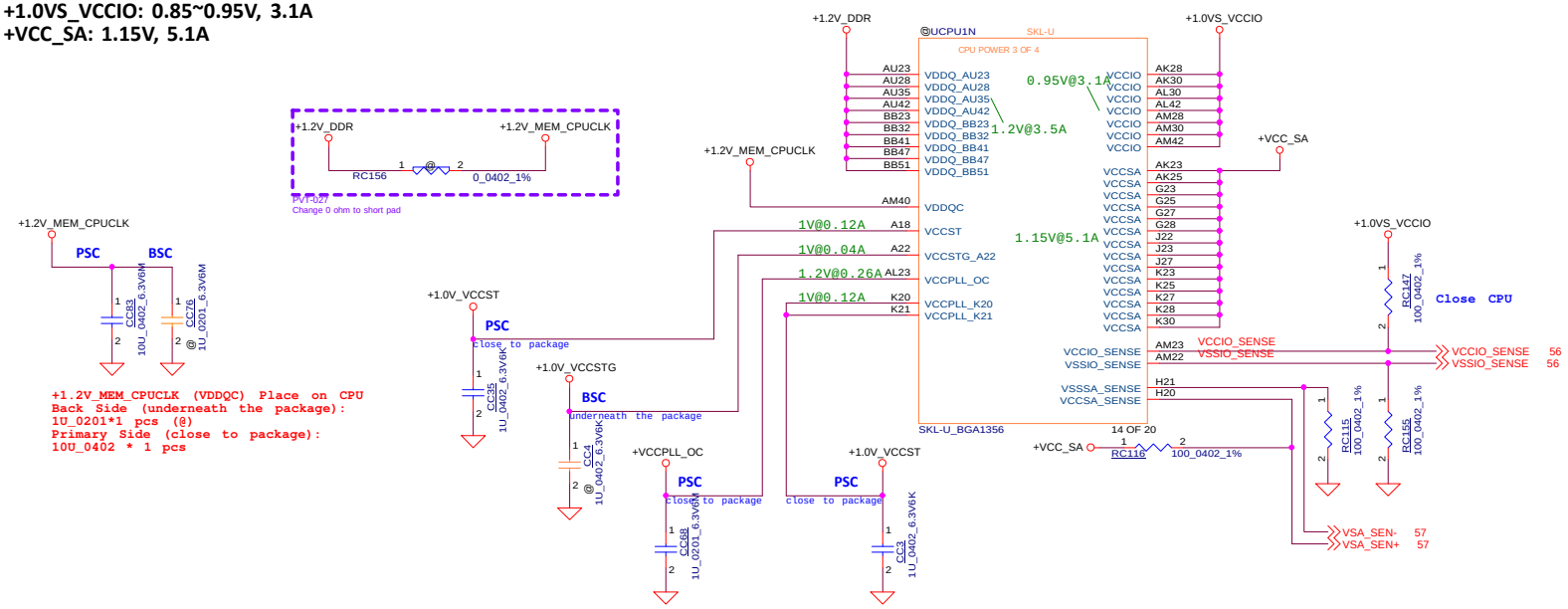
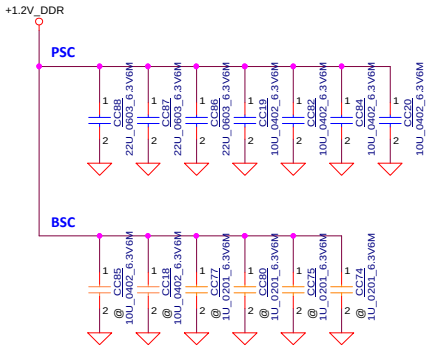
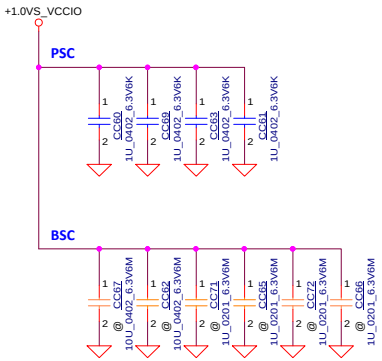
+1.2V_DDR: 1.2V, 3.5A
+1.0V_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA
+1.0V_VCCSTG: 1V, 40mA
+VCCPLL_OC: 1.2V, 260mA
+1.0VS_VCCIO: 0.85~0.95V, 3.1A
+VCC_SA: 1.15V, 5.1A



+1.2_DDR Decoupling Requirment
Back Side (underneath the package):
10U_0402*2 pcs + 1U_0201*4 pcs (@)
Primary Side (close to package):
10U_0402*4 pcs + 22U_0603*3 pcs



+1.0VS_VCCIO Decoupling Requirment
Back Side (underneath the package):
10U_0402*2 pcs + 1U_0201*4 pcs (@)
Primary Side (close to package):
1U_0402*4 pcs



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Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P16-MCP(12/14)PWR-VCCIO,MEM

Size	Document Number	Rev
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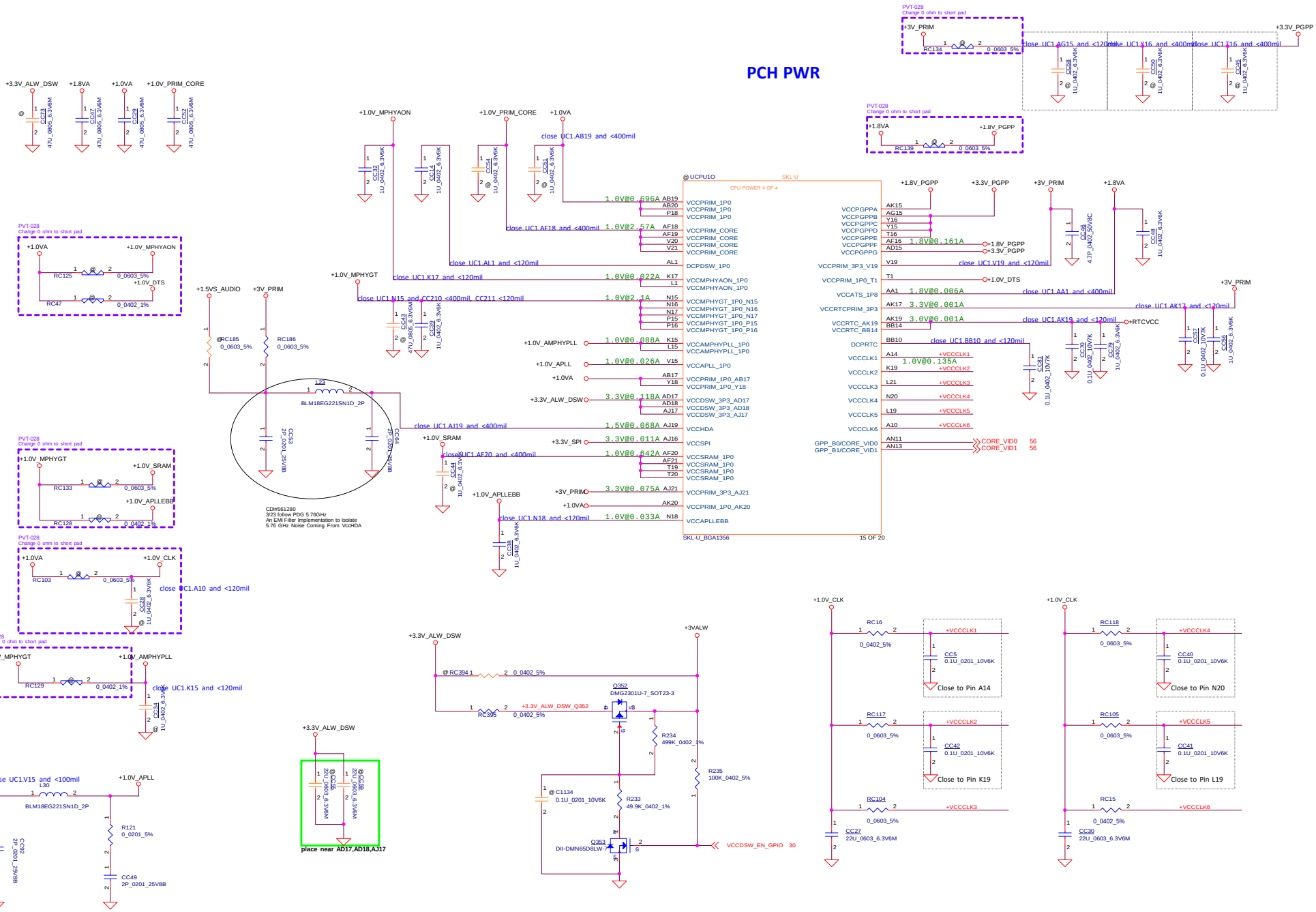
PCH PWR



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Title: P17-MCP(13/14)PCH PWR

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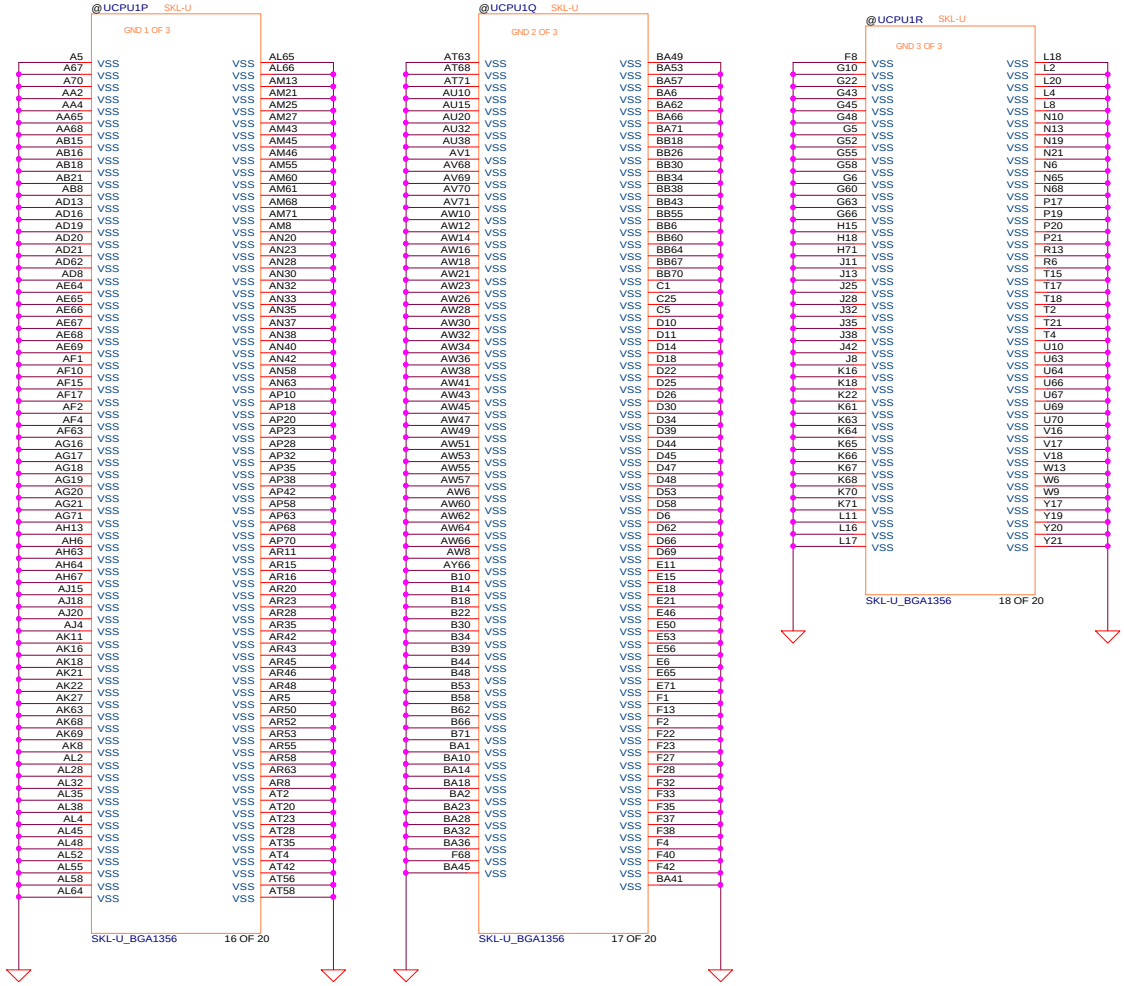

Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424

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Title: P18-MCP(14/14)VSS

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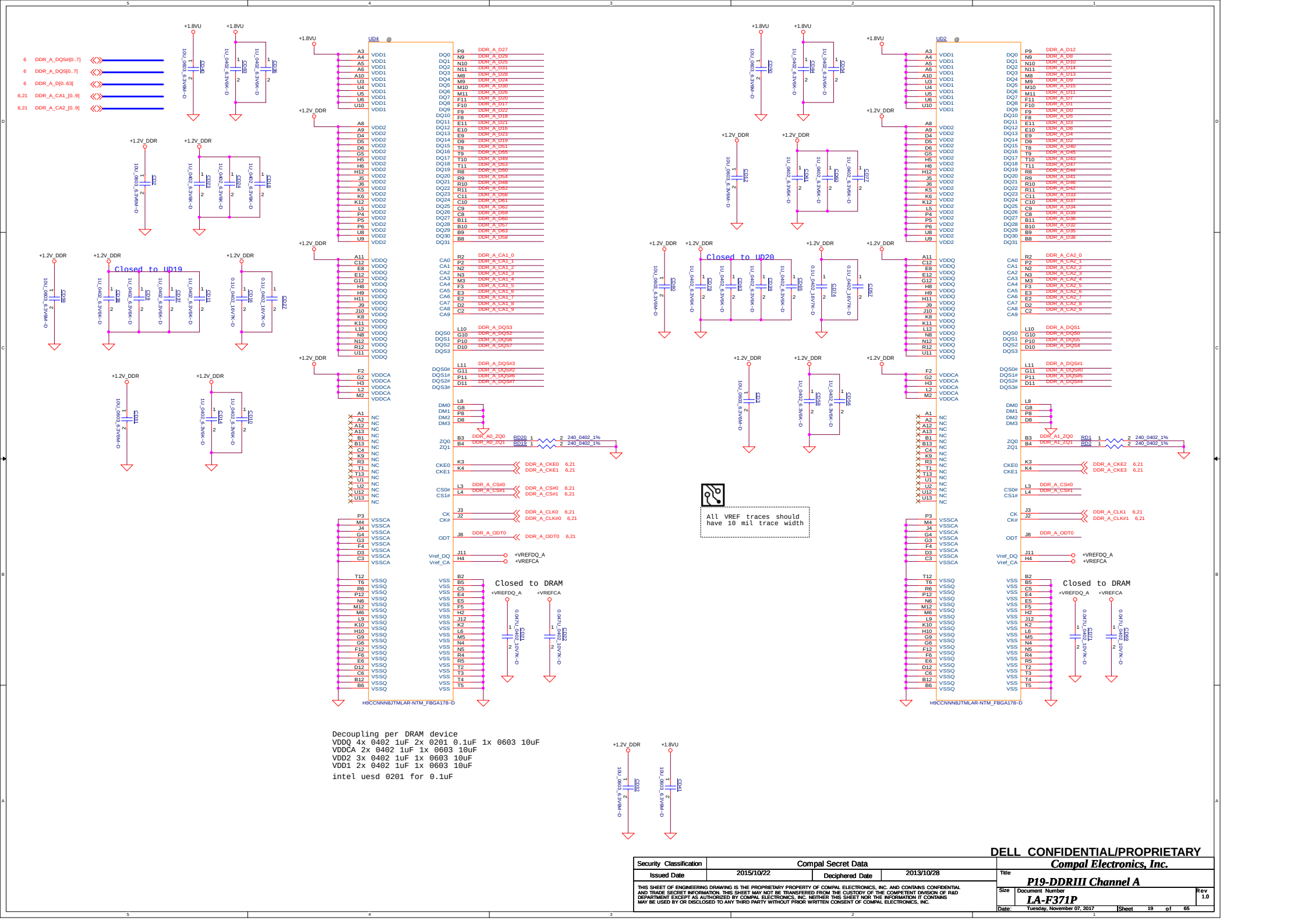

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Compal Electronics, Inc.

Title: P19-DDRIII Channel A

Size	Document Number	Rev
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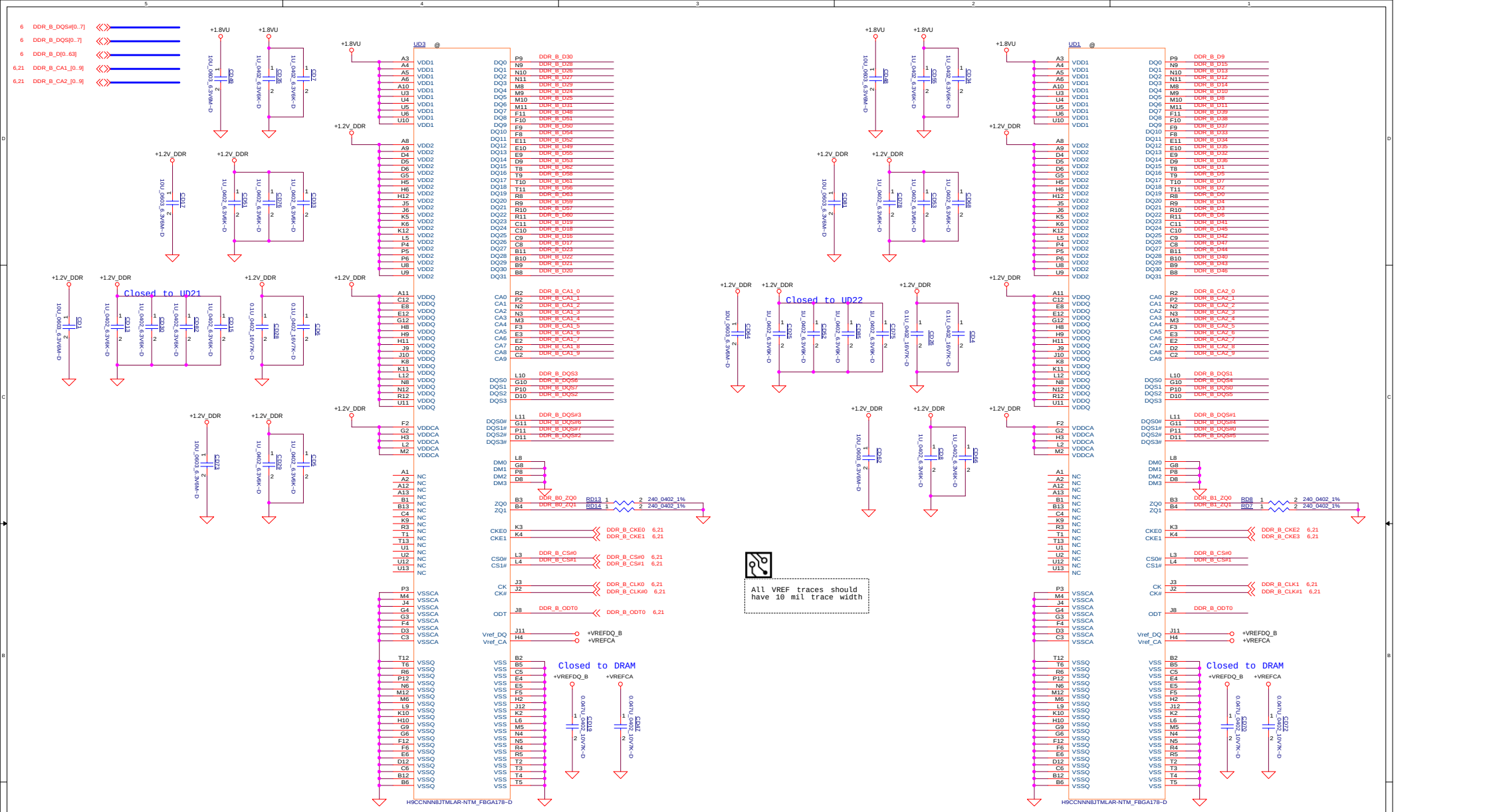

Decoupling per DRAM device
VDDQ 4x 0402 1uF 2x 0201 0.1uF 1x 0603 10uF
VDDCA 2x 0402 1uF 1x 0603 10uF
VDD2 3x 0402 1uF 1x 0603 10uF
VDD1 2x 0402 1uF 1x 0603 10uF

intel uesd 0201 for 0.1uF

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Compal Electronics, Inc.

Title: P20-DDRIII Channel B

Size	Document Number	Rev
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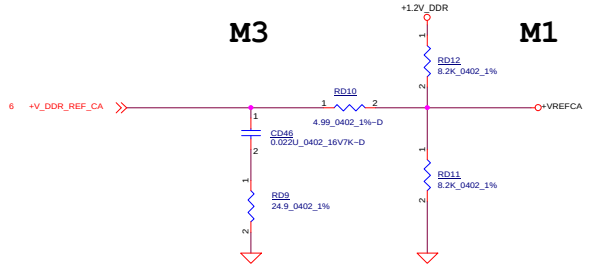
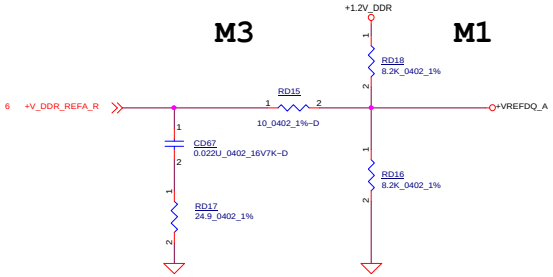
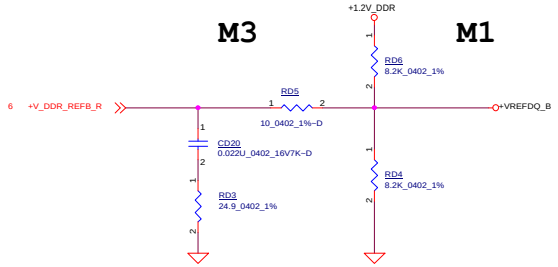
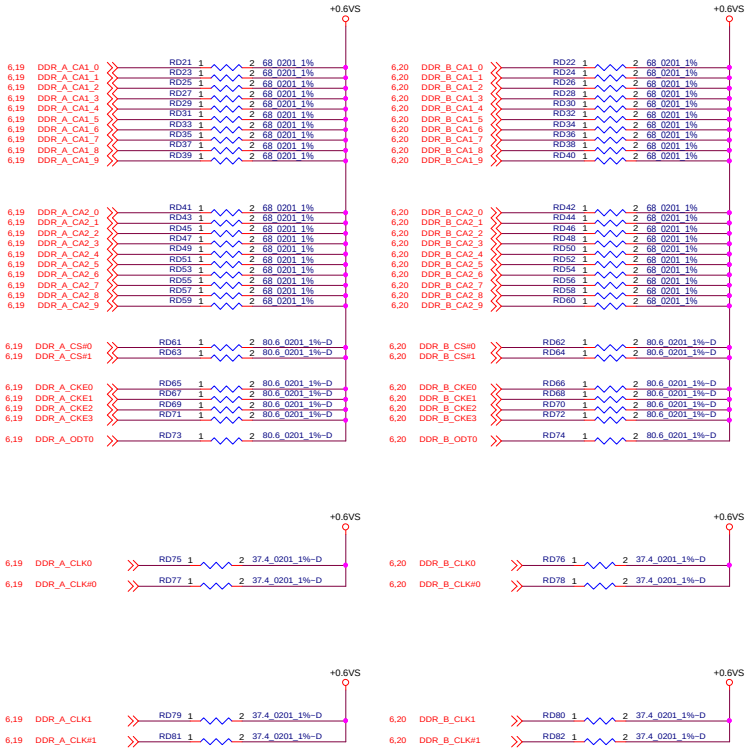
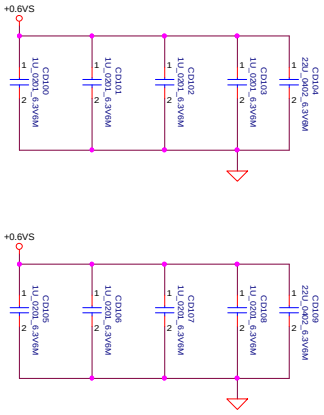
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.











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Compal Electronics, Inc.

Title: P21-DDRIII Vref & Termination

Size	Document Number	Rev
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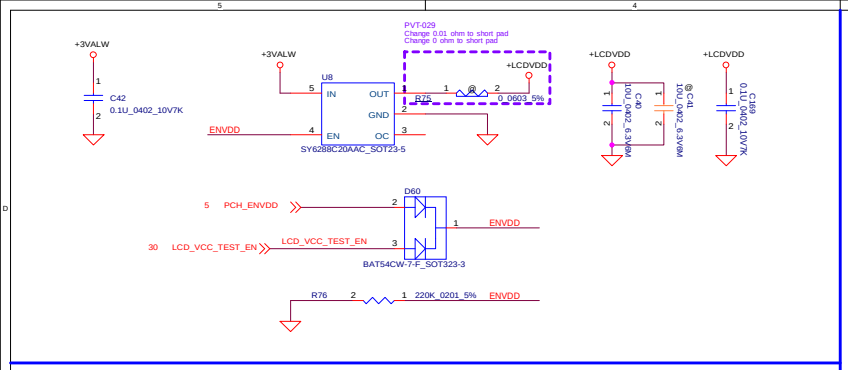
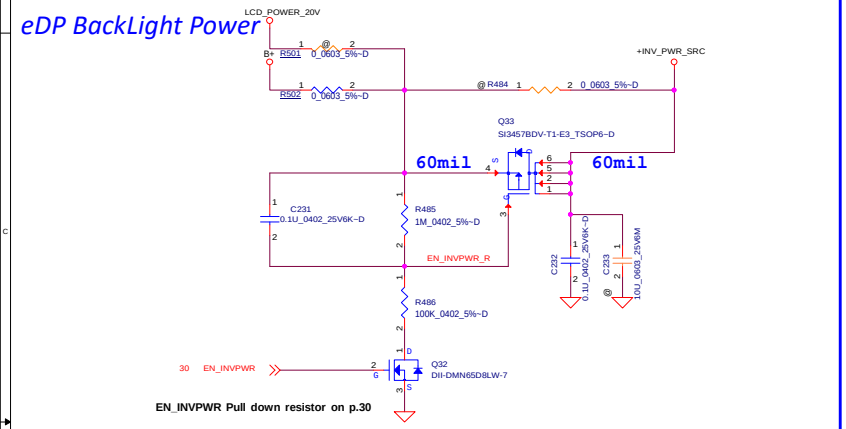
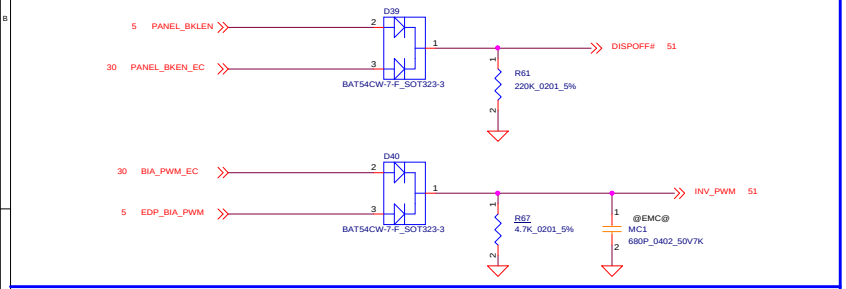


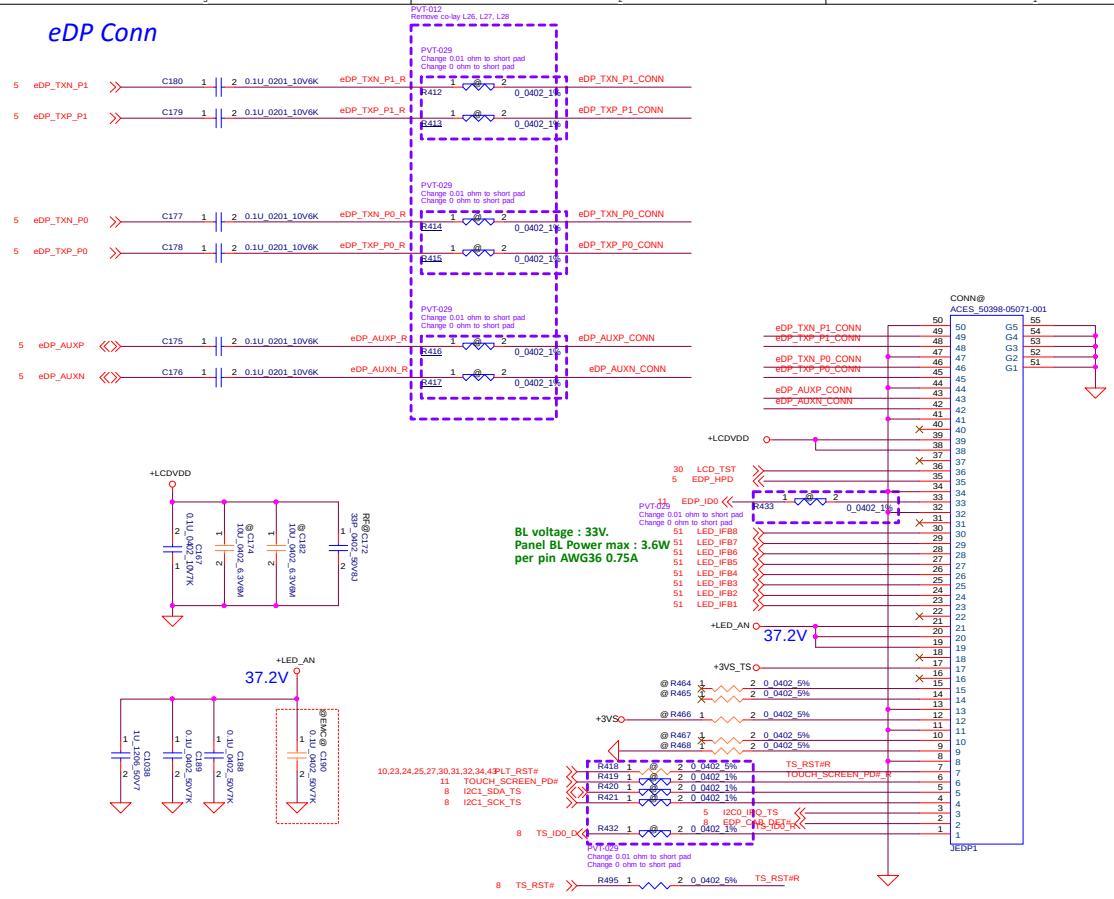
eDP BackLight Power



BackLight PWM Control

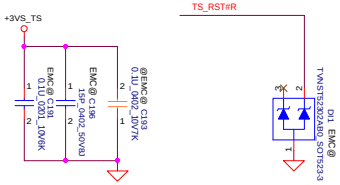


eDP Conn



Truth Table for EDP_ID/TS_ID0

Touch Controller	Panel	EDP_ID0	TS_ID0
TPK	SHARP	LOW	LOW
Laibao	SHARP	LOW	High
HH	BOE	High	LOW
Reserved		High	High



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Title: P22-eDP, TS

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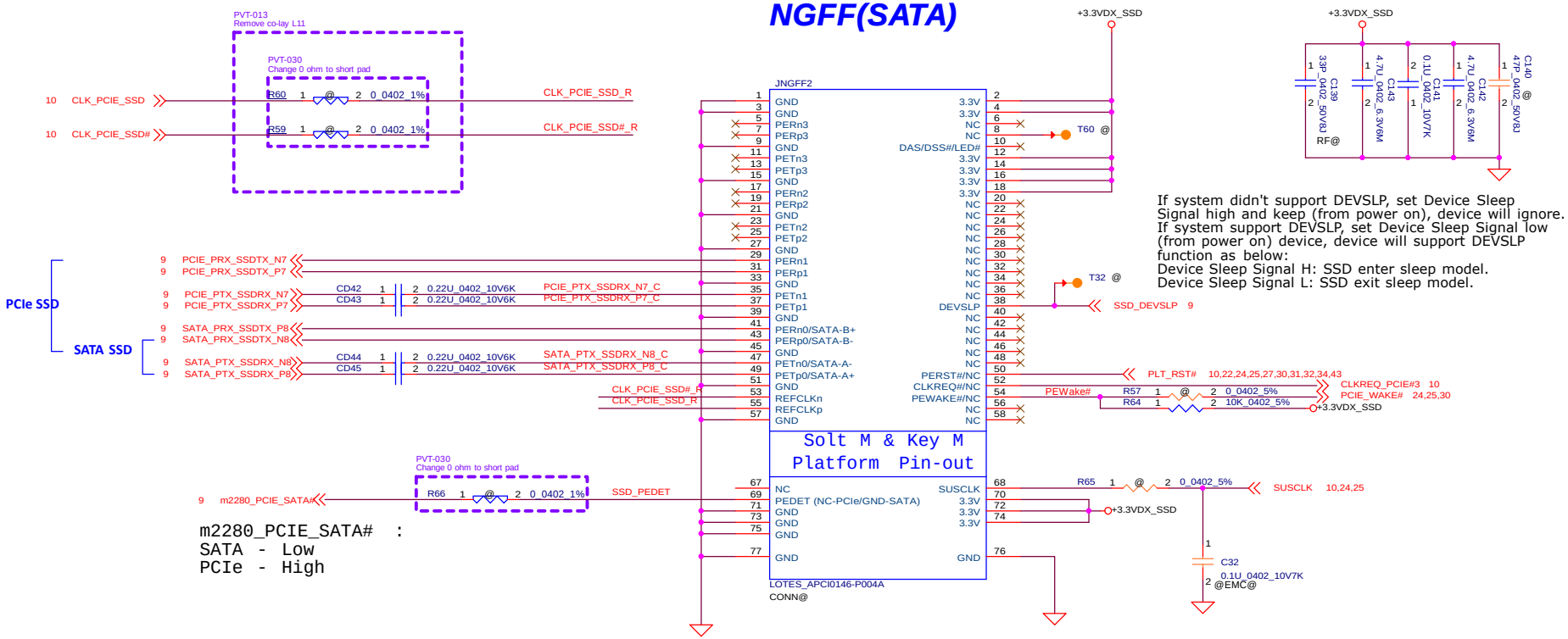

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Title: **P23-SATA / PCIE SSD**

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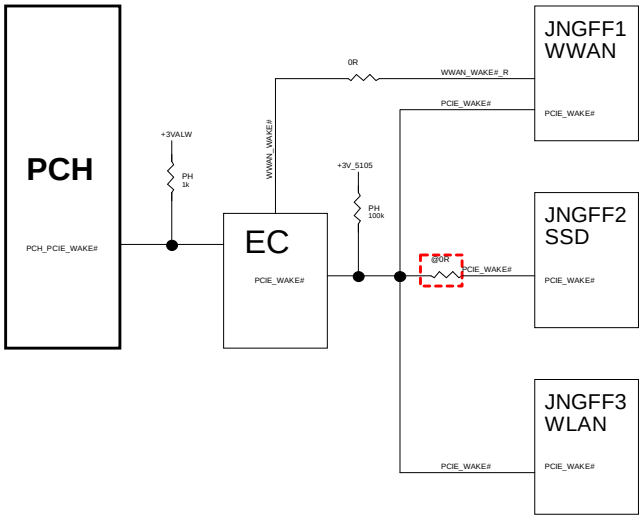
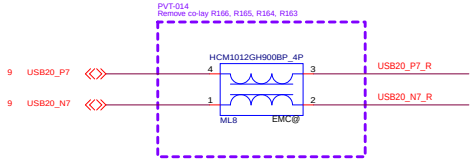
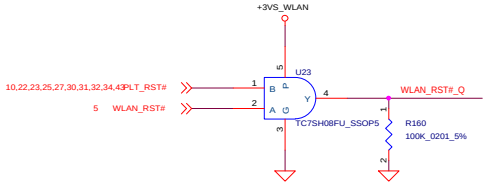
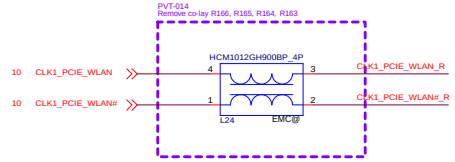
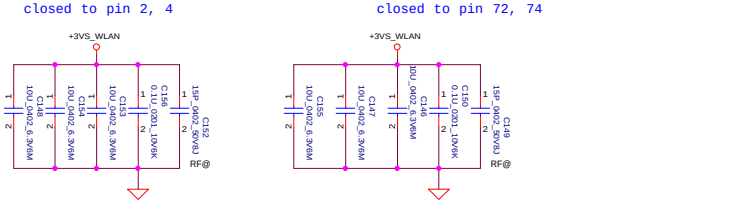
Wireless LAN

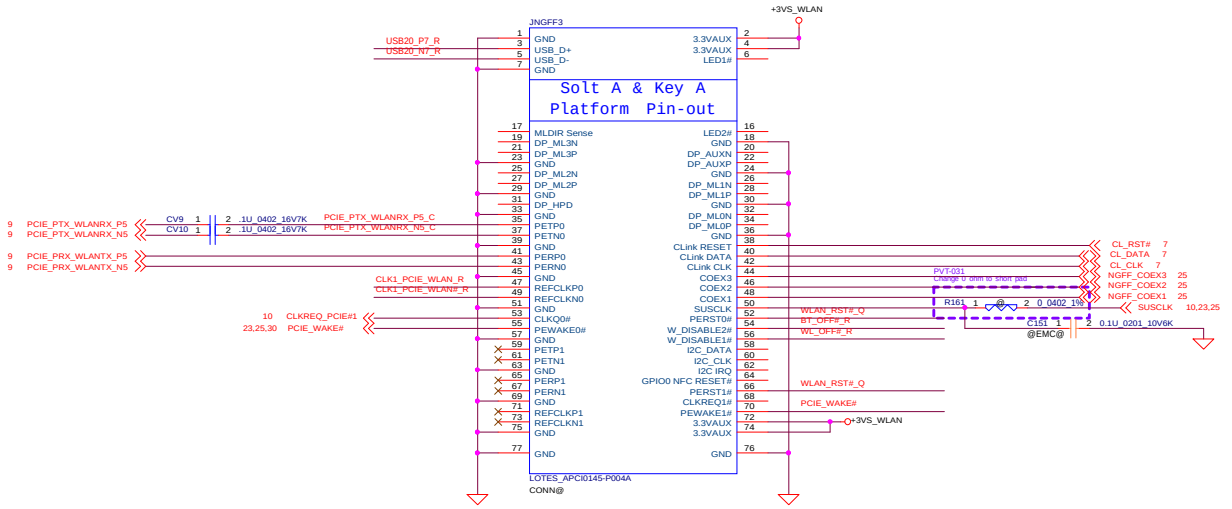


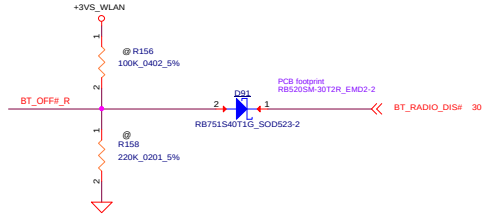


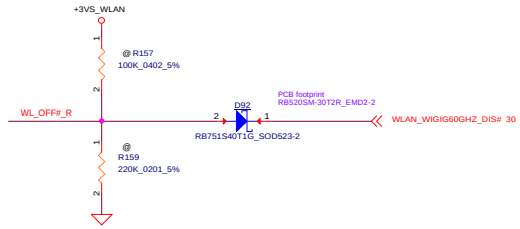












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Title: **P24-WLAN / BT**

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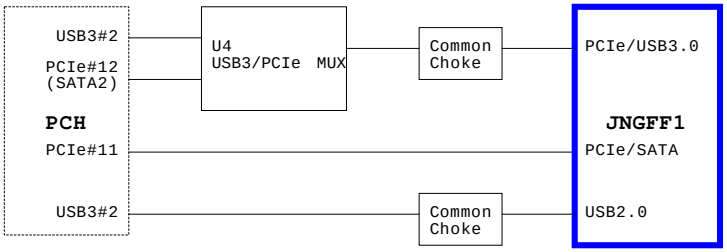

PCIe/USB 3.0 Mux

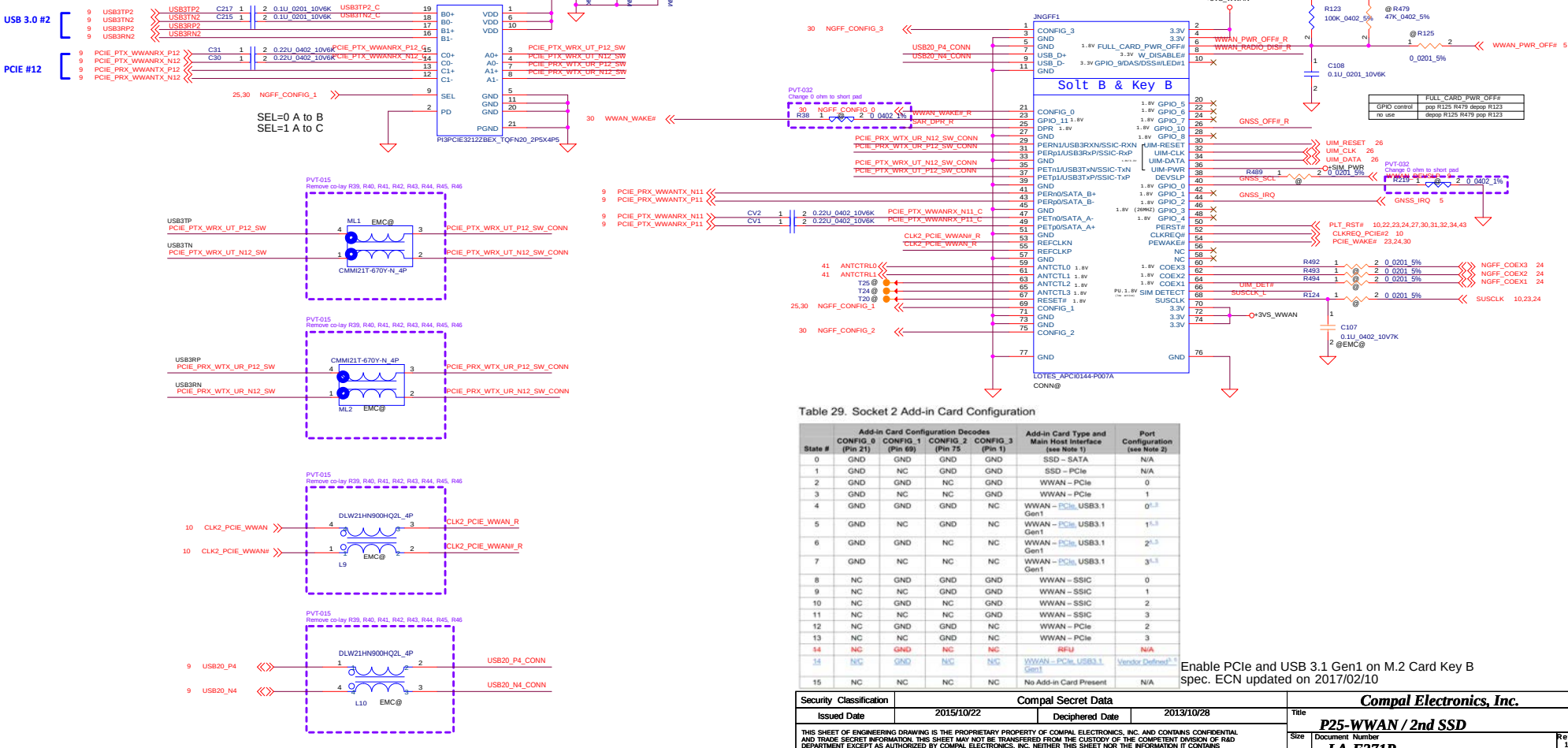

Table 29. Socket 2 Add-in Card Configuration

State #	Add-in Card Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Add-in Card Type and Main Host Interface (see Note 1)	Port Configuration (see Note 2)
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1
4	GND	GND	GND	NC	WWAN – PCIe, USB3.1 Gen1	0[1,3]
5	GND	NC	GND	NC	WWAN – PCIe, USB3.1 Gen1	1[1,3]
6	GND	GND	NC	NC	WWAN – PCIe, USB3.1 Gen1	2[1,3]
7	GND	NC	NC	NC	WWAN – PCIe, USB3.1 Gen1	3[1,3]
8	NC	GND	GND	GND	WWAN – SSIC	0
9	NC	NC	GND	GND	WWAN – SSIC	1
10	NC	GND	NC	GND	WWAN – SSIC	2
11	NC	NC	NC	GND	WWAN – SSIC	3
12	NC	GND	GND	NC	WWAN – PCIe	2
13	NC	NC	GND	NC	WWAN – PCIe	3
14	NC	GND	NC	NC	RFU	N/A
14	NC	GND	NC	NC	WWAN – PCIe, USB3.1 Gen1	Vendor Defined[3]
15	NC	NC	NC	NC	No Add-in Card Present	N/A

Enable PCIe and USB 3.1 Gen1 on M.2 Card Key B spec. ECN updated on 2017/02/10

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Title: **P25-WWAN / 2nd SSD**

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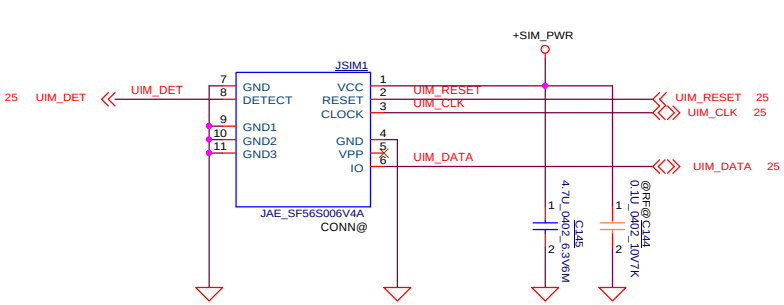
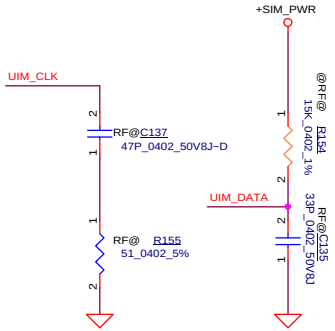
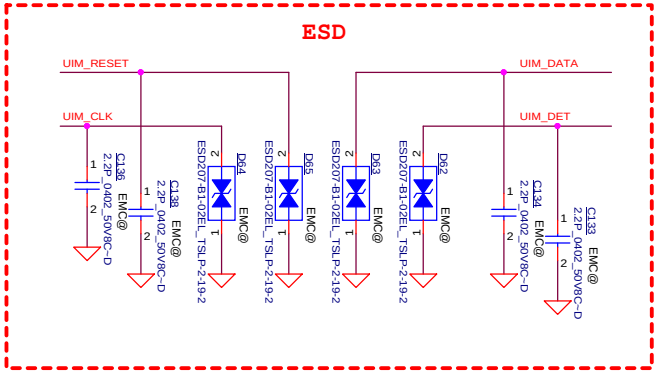
uSIM CONN



Normal Close





Compal Electronics, Inc.

Title: **P26-SIM Card CONN**

Size | Document Number: **LA-F371P** | Rev: 1.0

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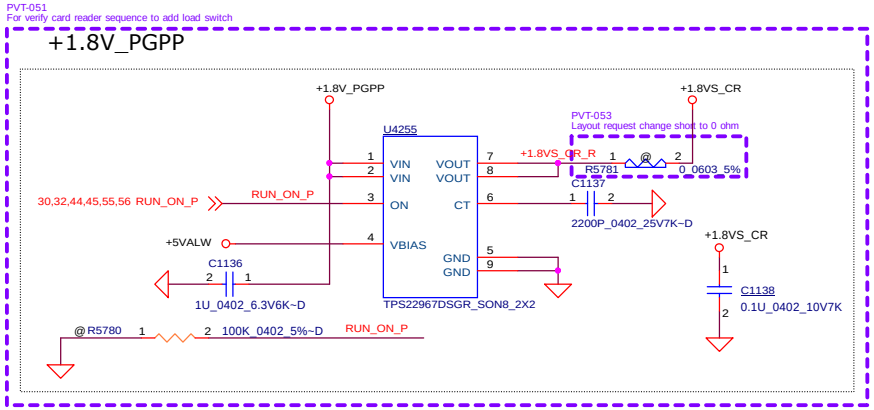
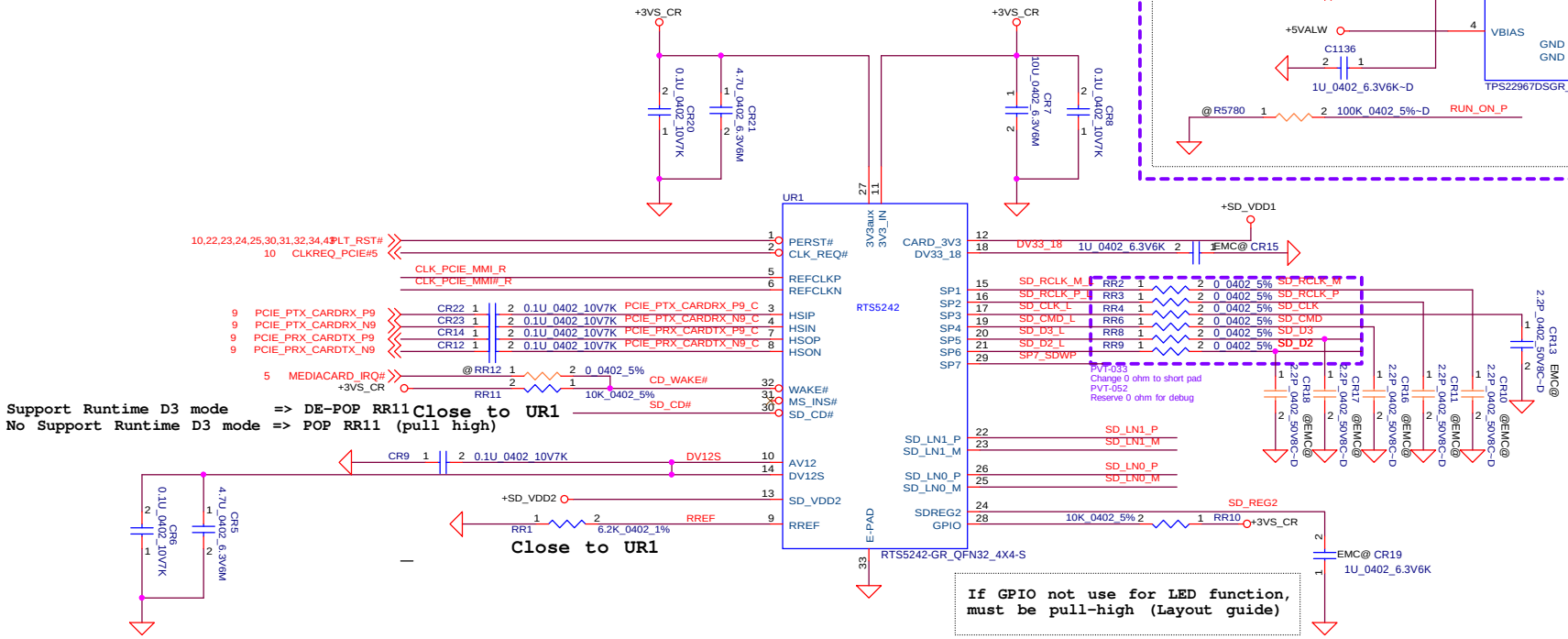
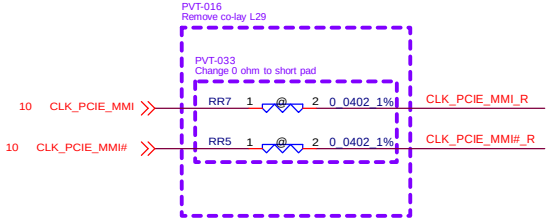
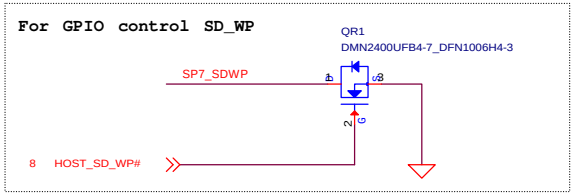
Card Reader

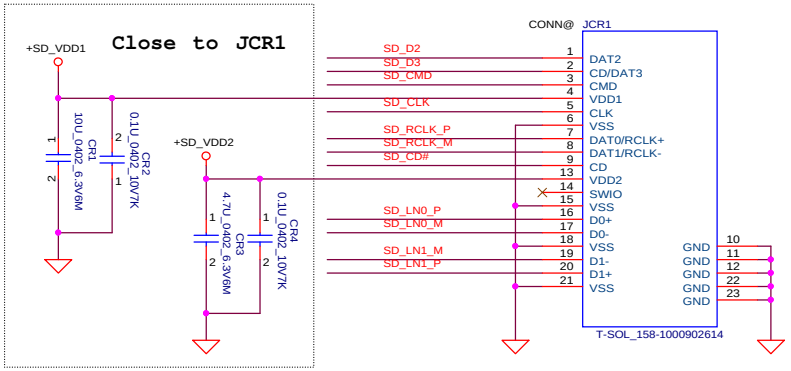
1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
   - Bulk capacitor for Card_3V3 place closed to flash card socket.
   - Bulk capacitor for 3V3_IN / 3V3aux / DV12S place closed to RTS5242 chip.
3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.











Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P27-Card Reader(RT5242)**

Size	Document Number	Rev
		1.0

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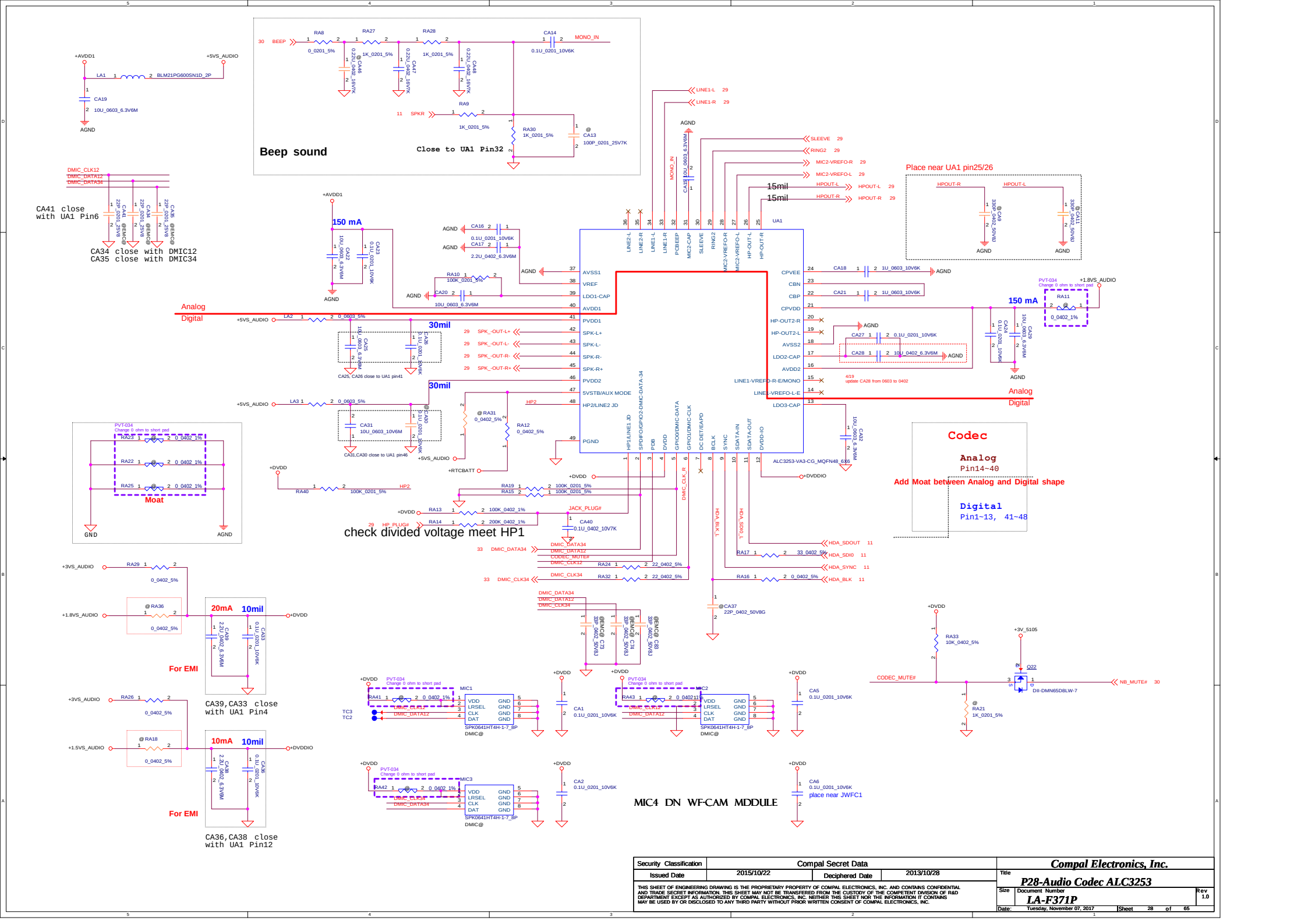
Beep sound
Close to UA1 Pin32
CA41 close with UA1 Pin6
CA34 close with DMIC12
CA35 close with DMIC34
Analog
Digital
30mil
check divided voltage meet HP1
Moat
For EMI
CA39,CA33 close with UA1 Pin4
CA36,CA38 close with UA1 Pin12
MIC4 DN WF-CAM MDDULE
Place near UA1 pin25/26
15mil
Codec
Analog
Pin14~40
Add Moat between Analog and Digital shape
Digital
Pin1~13, 41~48
ALC3253-VA3-CG_MQFN48_6X6
Security Classification
Compal Secret Data
Issued Date
2015/10/22
Deciphered Date
2013/10/28
Compal Electronics, Inc.
P28-Audio Codec ALC3253
LA-F371P
Tuesday, November 07, 2017
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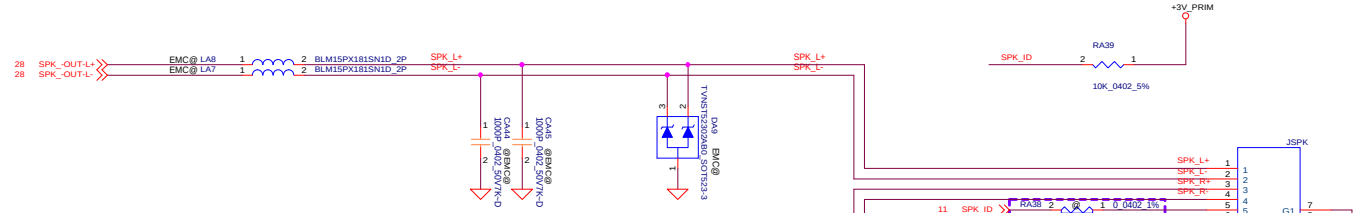
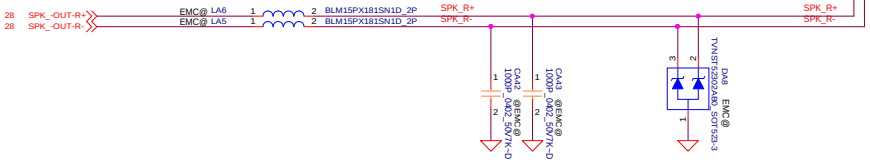
Int. Speaker Conn.

40mil = For 4ohm 3W Speaker



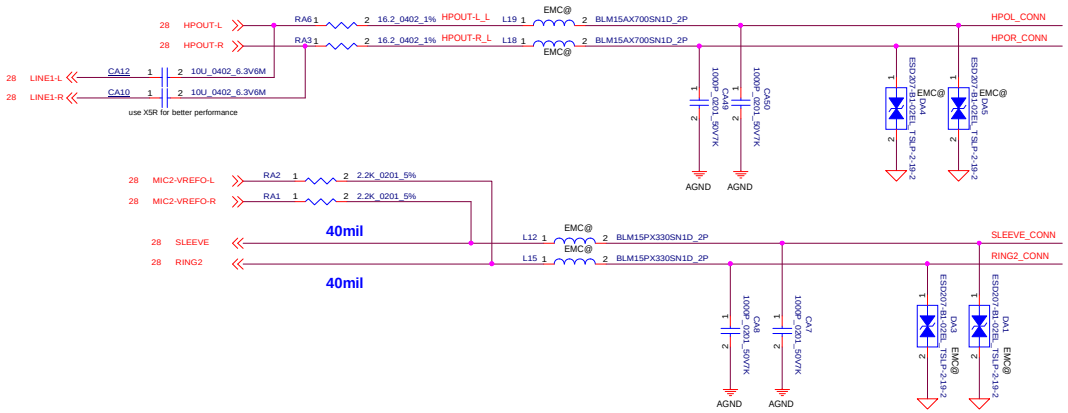
Int. Speaker Conn.

40mil = For 4ohm 3W Speaker

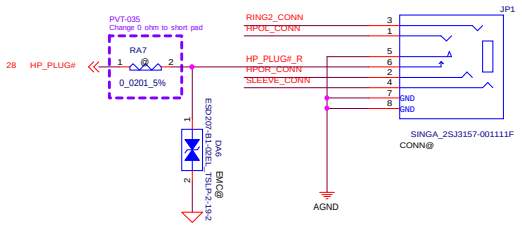


SPK_ID	Speaker
High	Main Soure
Low	2nd Soure

Universal Audio Jack



Universal Audio Jack CONN



Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P29-SPK CONN**

Size	Document Number	Rev
	LA-F371P	1.0

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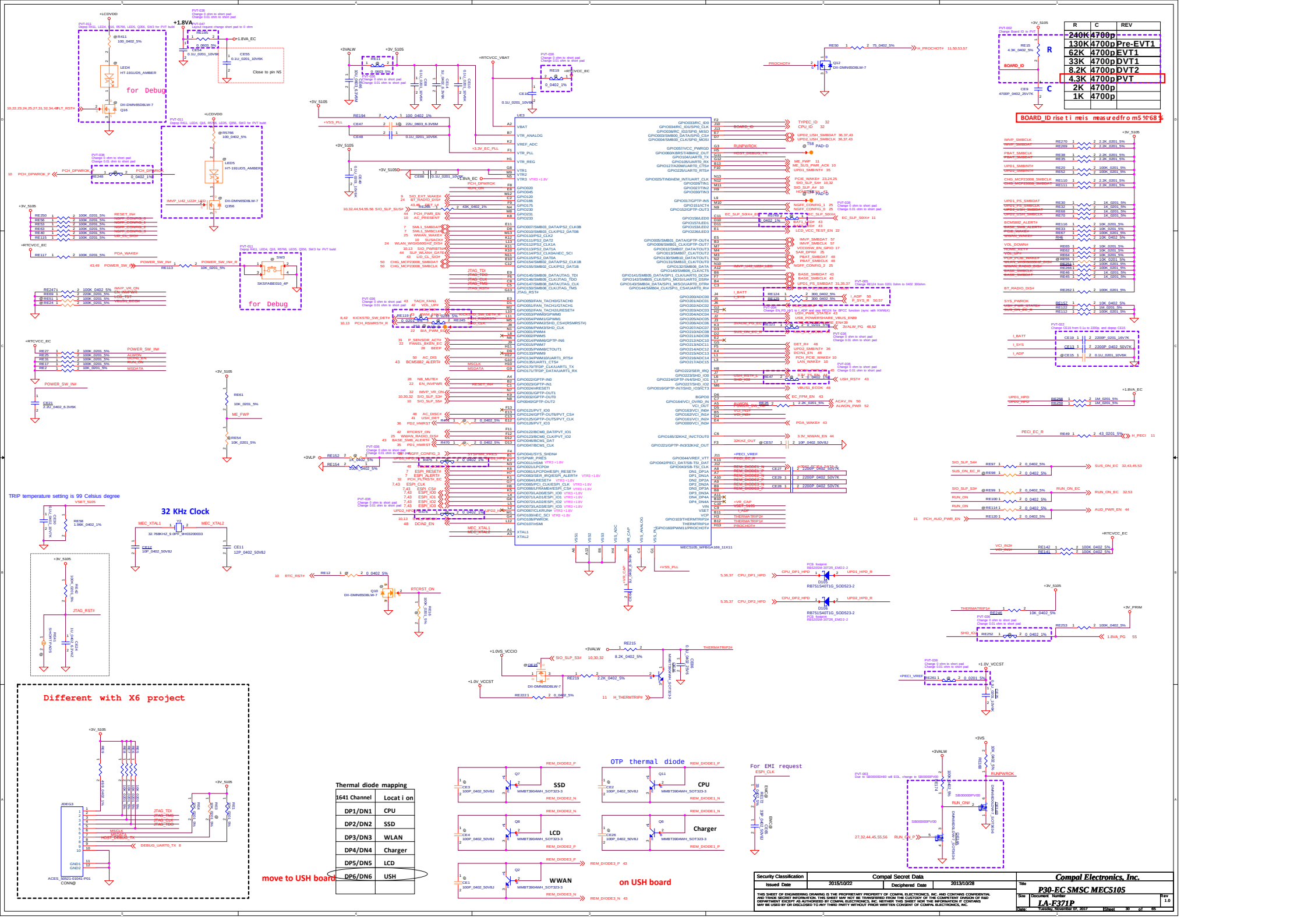
for Debug
for Debug
TRIP temperature setting is 99 Celsius degree
32 KHz Clock
Different with X6 project
move to USH board
on USH board
OTP thermal diode
For EMI request
SSD
CPU
LCD
Charger
WWAN
BOARD_ID rise ti meis measuredfro m5 %~68 %
R C REV
240K 4700p
130K 4700p Pre-EVT1
62K 4700p EVT1
33K 4700p DVT1
8.2K 4700p DVT2
4.3K 4700p PVT
2K 4700p
1K 4700p
Thermal diode mapping
1641 Channel Locat i on
DP1/DN1 CPU
DP2/DN2 SSD
DP3/DN3 WLAN
DP4/DN4 Charger
DP5/DN5 LCD
DP6/DN6 USH
Security Classification
Compal Secret Data
Issued Date 2015/10/22
Deciphered Date 2013/10/28
Compal Electronics, Inc.
P30-EC SMSC MEC5105
LA-F371P
Rev 1.0
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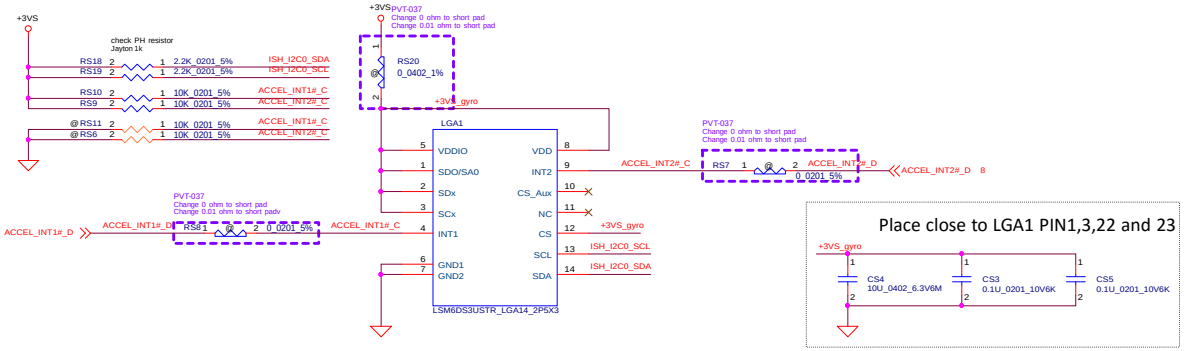
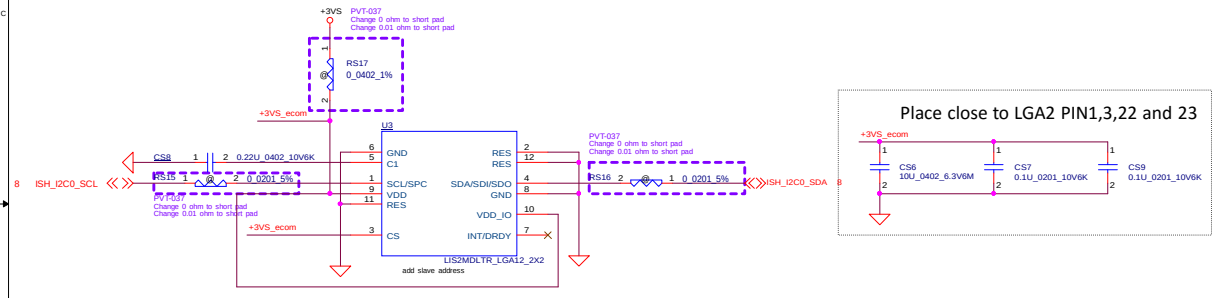
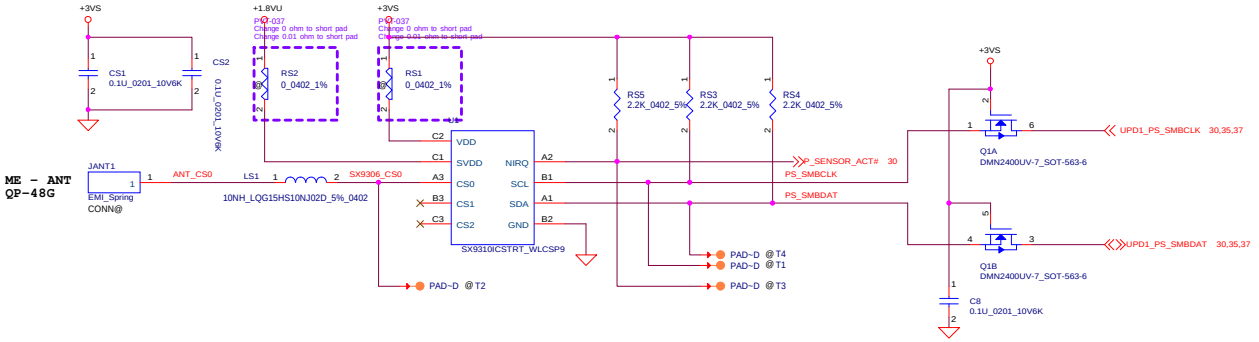
Gyro + Accelerometer



E-Compass

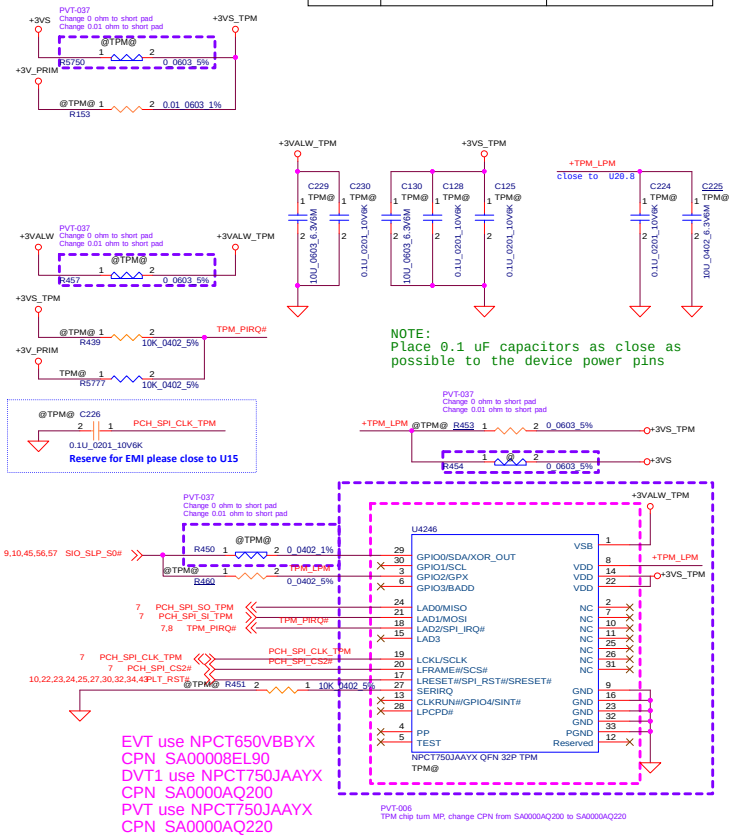


SAR Proximity Sensor



TPM

	Pop	De-pop
NPCT65x	R153, R451, R460	R5750, R450
* NPCT75x	R5750, R450	R153, R451, R460



Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P31-Sensor / TPM**

Size	Document Number	Rev
	LA-F371P	1.0

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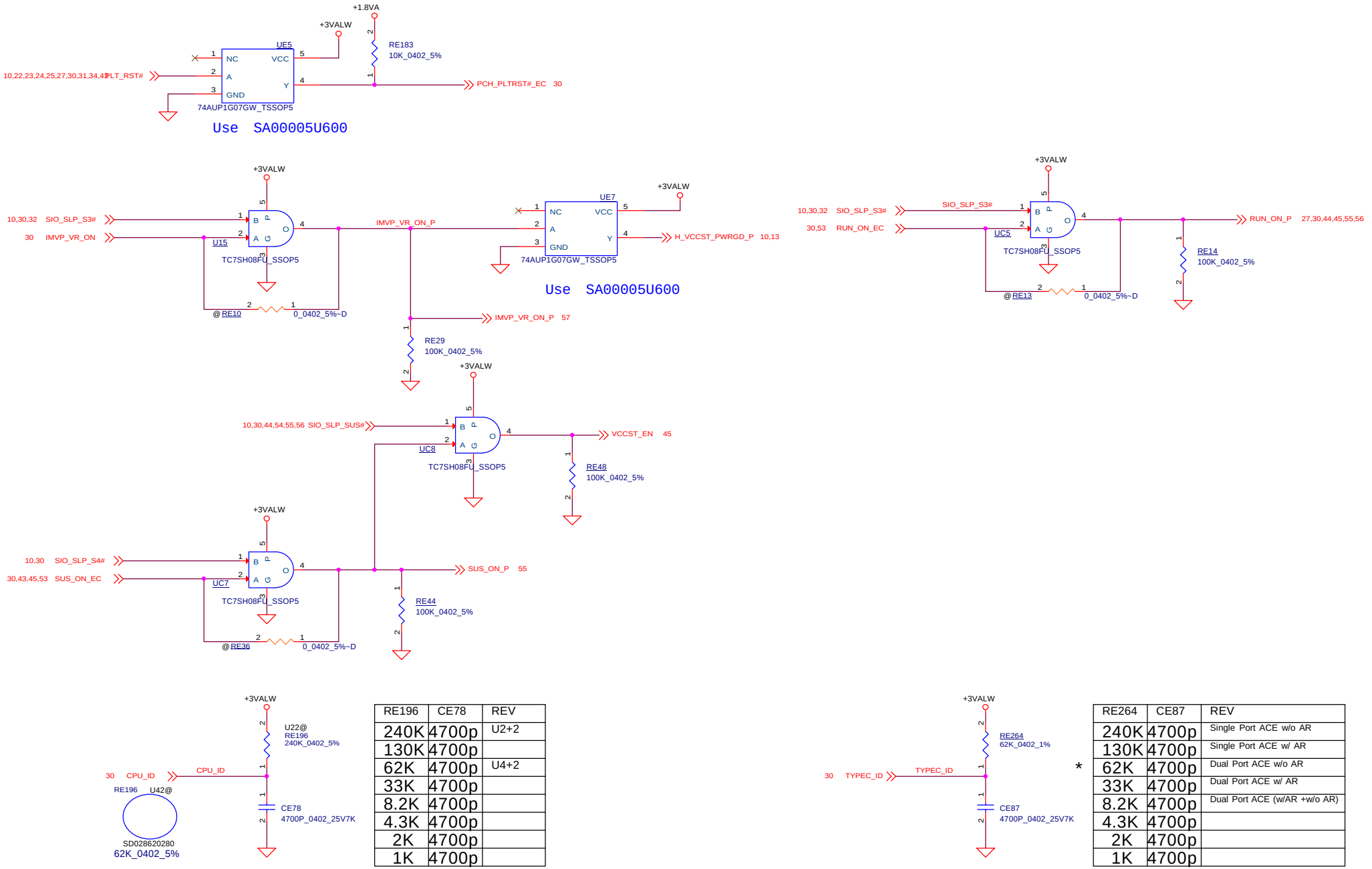

RE196	CE78	REV
240K	4700p	U2+2
130K	4700p	
62K	4700p	U4+2
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

*

RE264	CE87	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/ AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/ AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P32-PWRGD**

Size | Document Number: **LA-F371P** | Rev: 1.0

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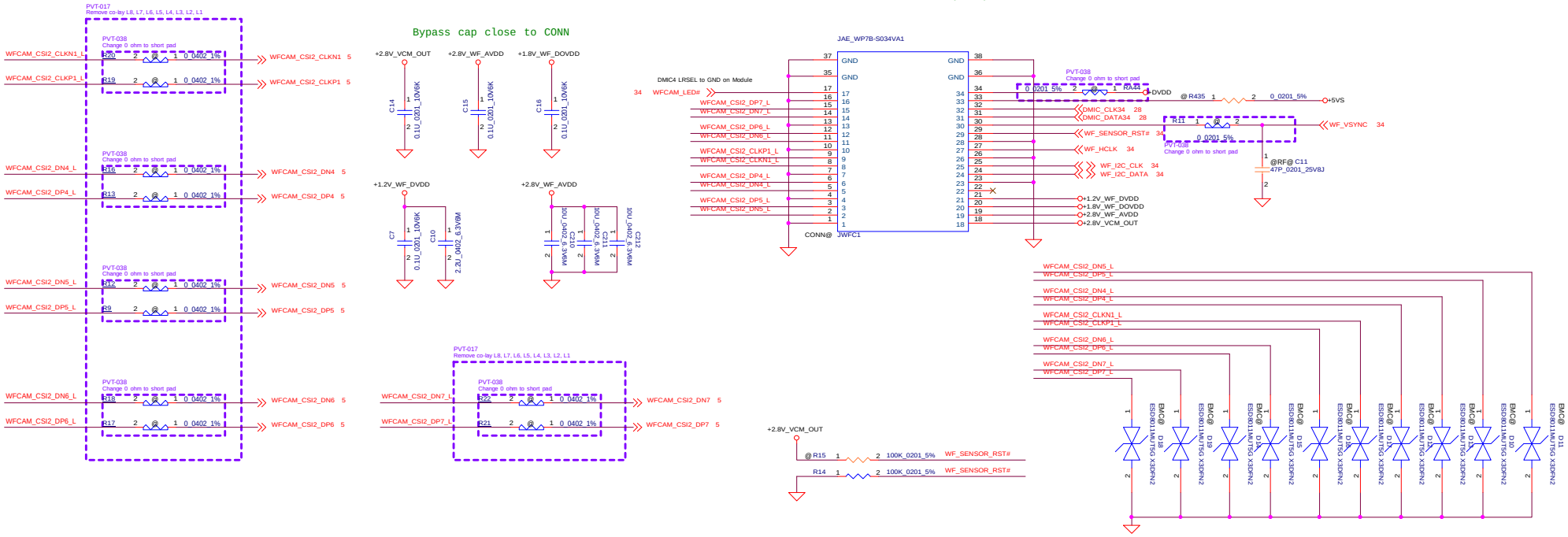
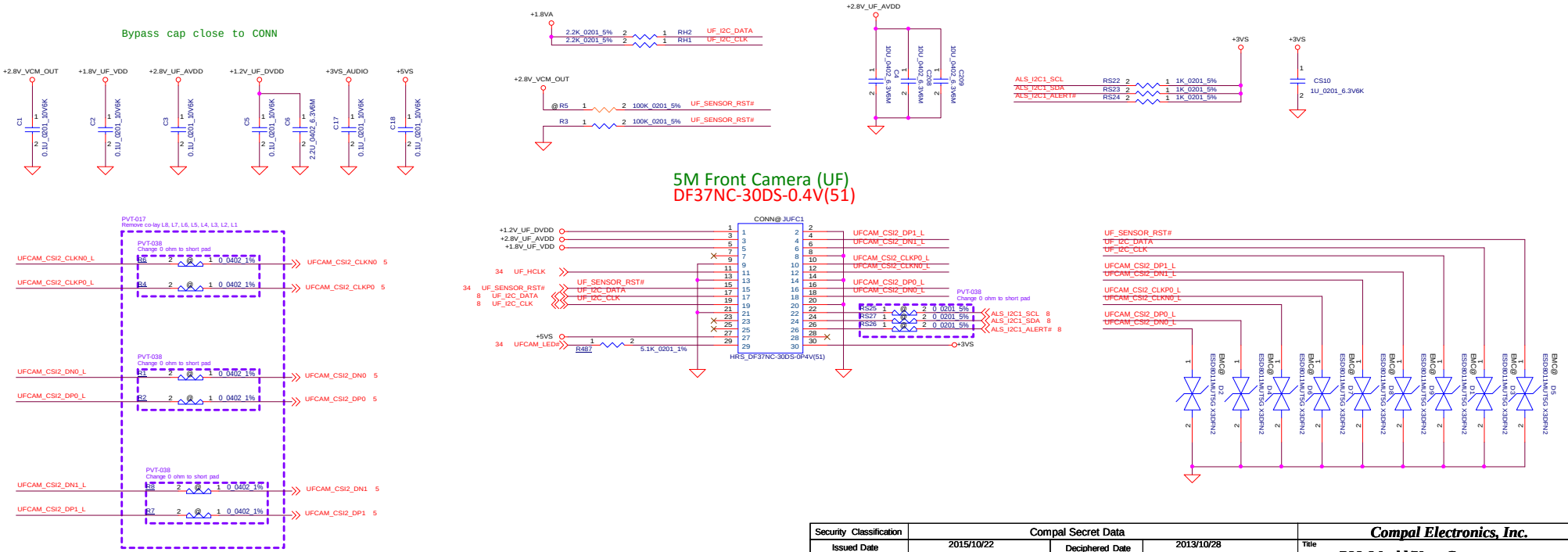
8M Rear Camera (WF)



5M Front Camera (UF)
DF37NC-30DS-0.4V(51)



Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P33-World/User Camera**

Size	Document Number	Rev
	LA-F371P	1.0

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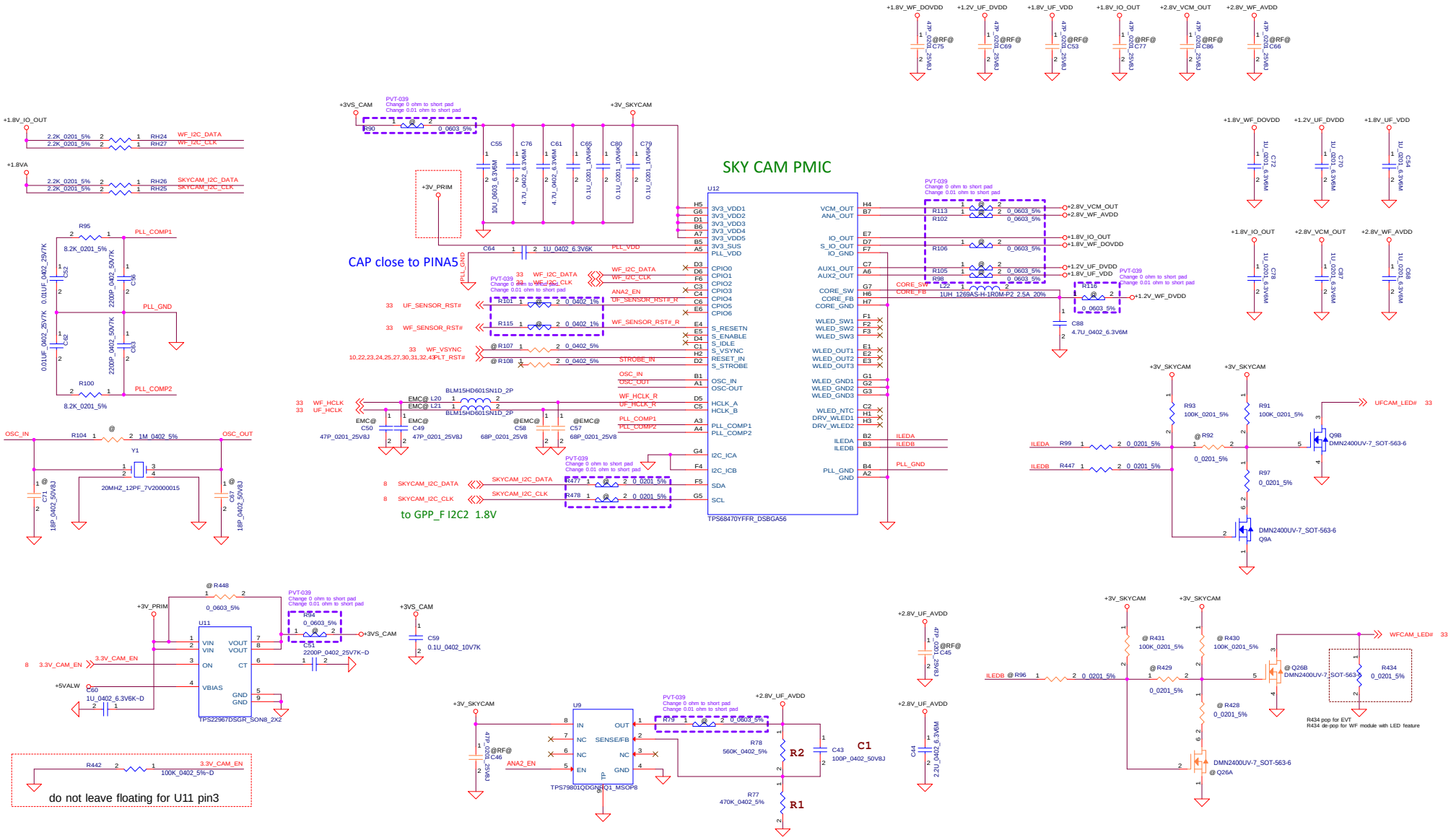

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **P34-Camera PMIC**

Size	Document Number	Rev
	LA-F371P	1.0

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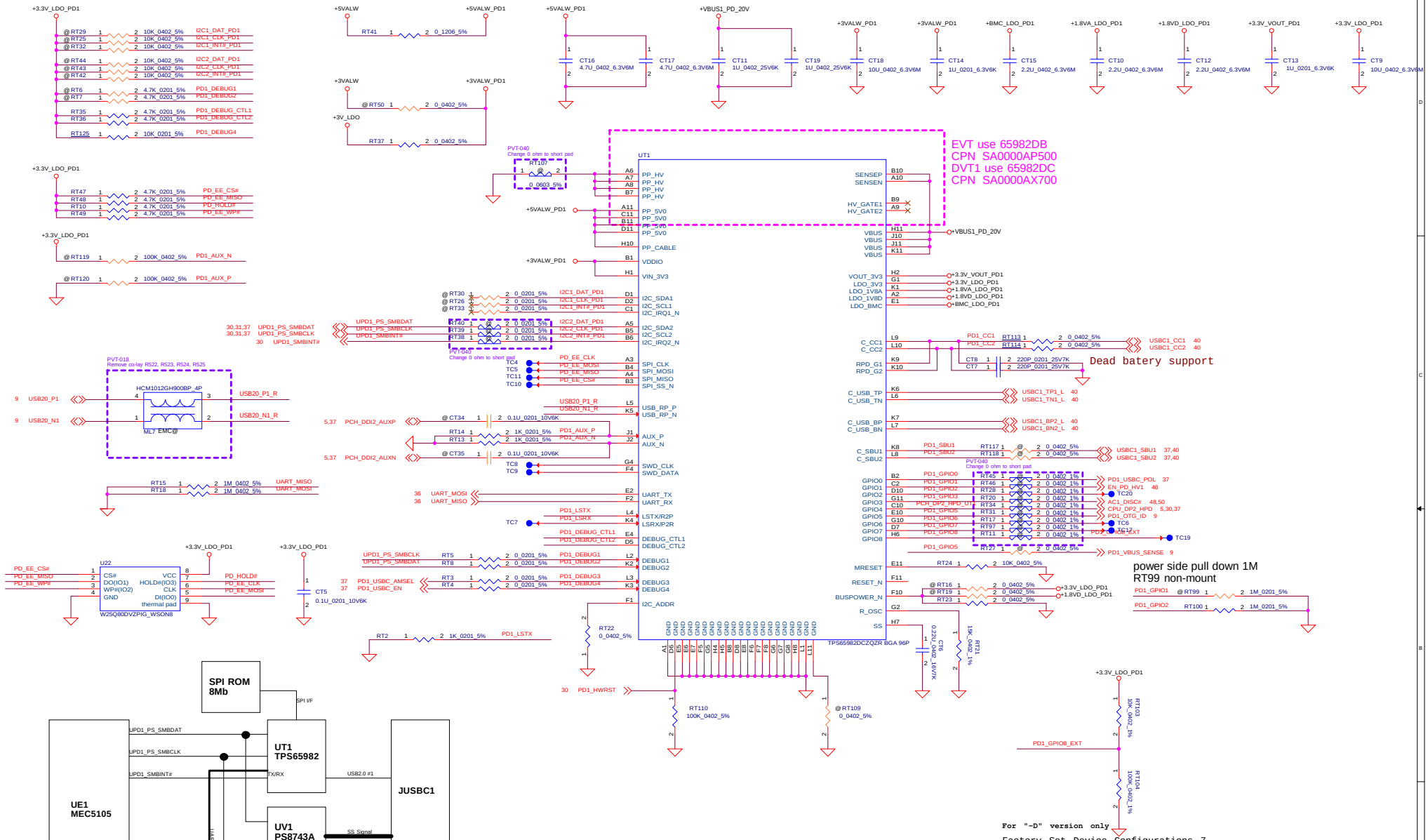

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **P35-PD Controller TI**

Size	Document Number	Rev
C	LA-F371P	1.0

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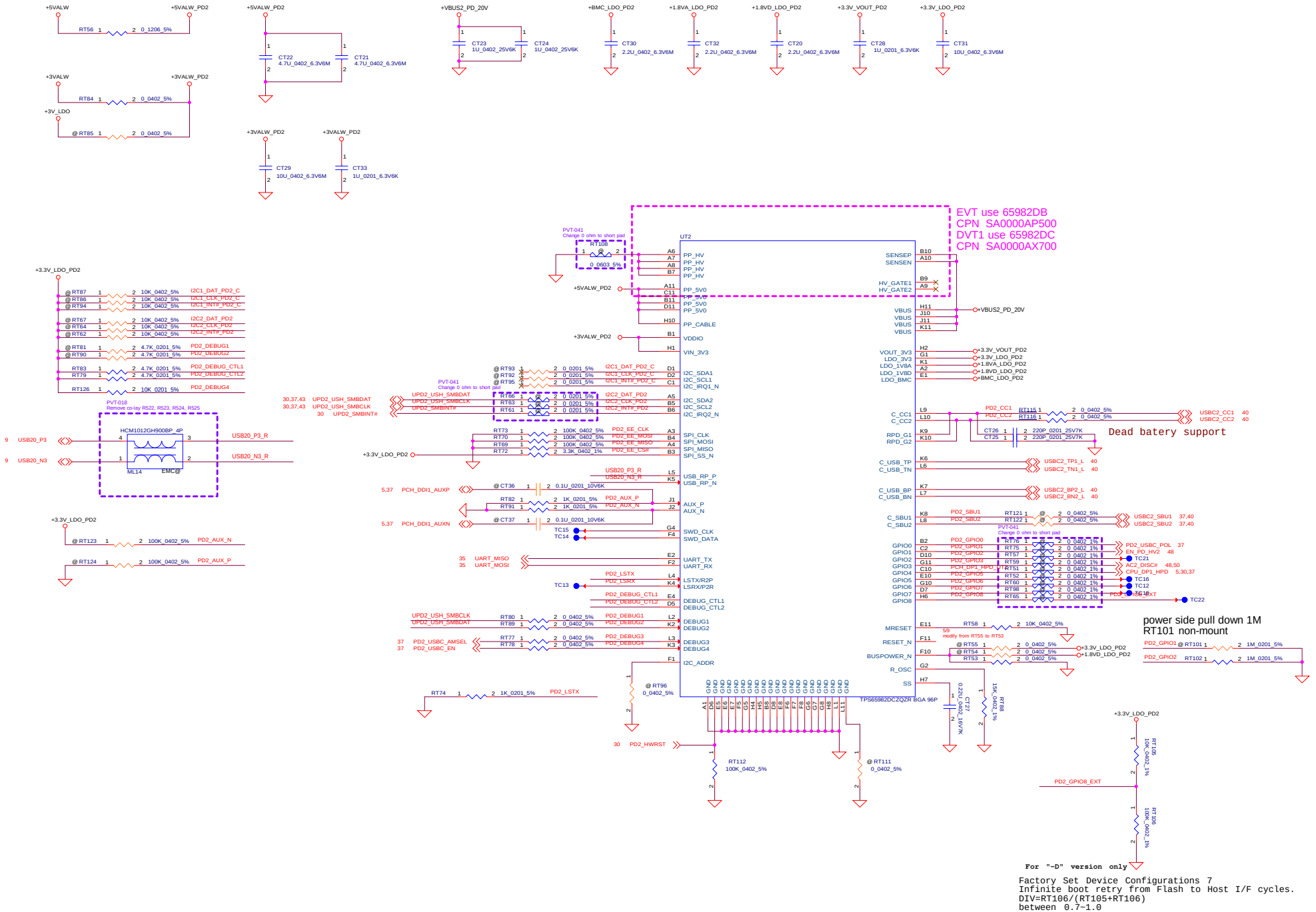

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: **P36-PD Controller TI**

Size	Document Number	Rev
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RV26 pop and RV14 de-pop for PS8743A
RV26 de-pop and RV14 pop for PS8743B

close to UV1

close to UV1 pin17

ADDR=High

Deafult use I2C

EVT use PS8743A_B0
CPN SA00009YO00
DVT1 use PS8743A_B1
CPN SA00009YO10

USBC1 MUX default H/W setting

CE_DP	CE_USB	FLIP	TUSB546 Configuration	USB4 Display Port Alt Mode DFP_D Configuration
L	L	L	Power Down	
L	L	H	Power Down	
L	H	L	One Port USB 3.1 - No Flip	
L	H	H	One Port USB 3.1 - With Flip	
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP - With Flip	C and E
H	H	L	One Port USB 3.1 + 2Lane DP -No Flip	D and F
H	H	H	One Port USB 3.1 + 2Lane DP -With Flip	D and F

USB 3.0 AC Coupling Capacitor Topology

PCH DDI2
PCH
PCH DDI1

USB-C Port-A
MUX+Redriver UV1
USB-C RECEPTACLE

USB-C Port-B
MUX+Redriver UV2
USB-C RECEPTACLE

close to UV2

close to UV2 pin17

ADDR=Low

Deafult use I2C

USBC2 MUX default H/W setting

CE_DP	CE_USB	FLIP	TUSB546 Configuration	USB4 Display Port Alt Mode DFP_D Configuration
L	L	L	Power Down	
L	L	H	Power Down	
L	H	L	One Port USB 3.1 - No Flip	
L	H	H	One Port USB 3.1 - With Flip	
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP - With Flip	C and E
H	H	L	One Port USB 3.1 + 2Lane DP -No Flip	D and F
H	H	H	One Port USB 3.1 + 2Lane DP -With Flip	D and F

PCH
UV1 PS8743A
UV2 PS8743A
UT1 TPS65982
UT2 TPS65982
MEC5105
JUSBC1
JUSBC2
BME dock

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

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Compal Electronics, Inc.

Title: P37-MUX Re-Driver

Size: D | Document Number: LA-F371P | Rev: 1.0

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Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P38-DDI WiGig MUX**

Size	Document Number	Rev
C	LA-F371P	1.0

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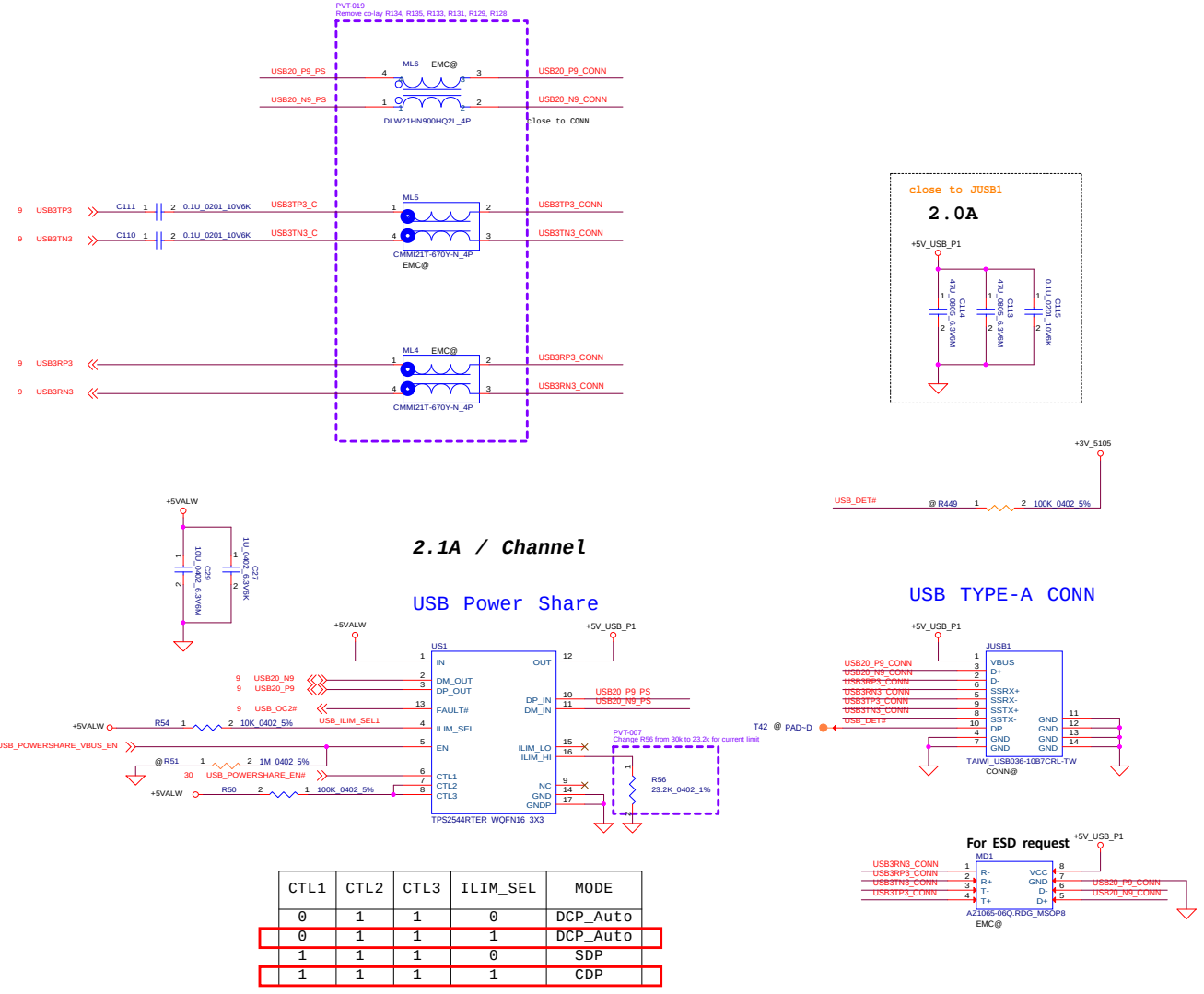

CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDP
1	1	1	1	CDP

Compal Electronics, Inc.

Title: P39-VUBS Provider-Type-A

Size: C | Document Number: LA-F371P | Rev: 1.0

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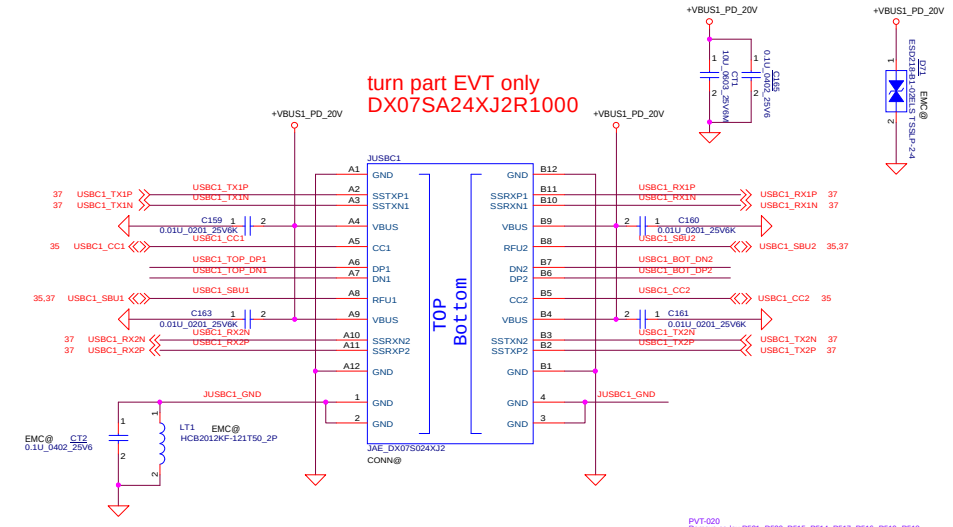
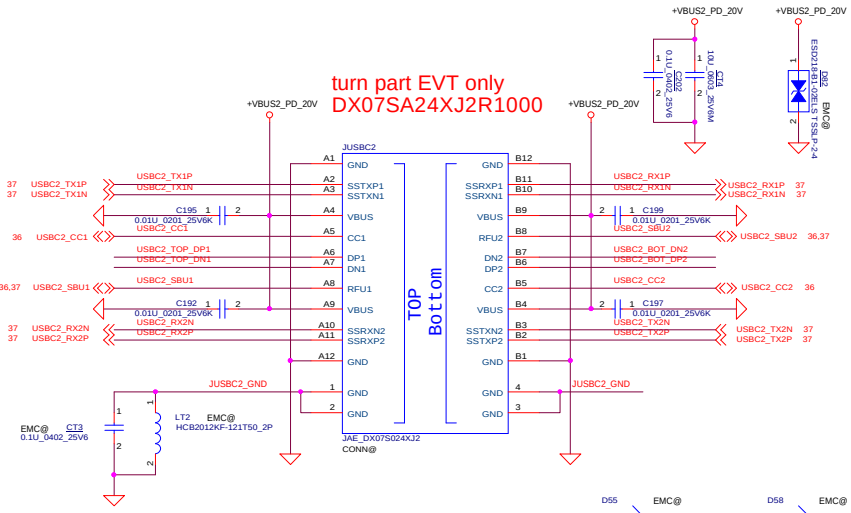
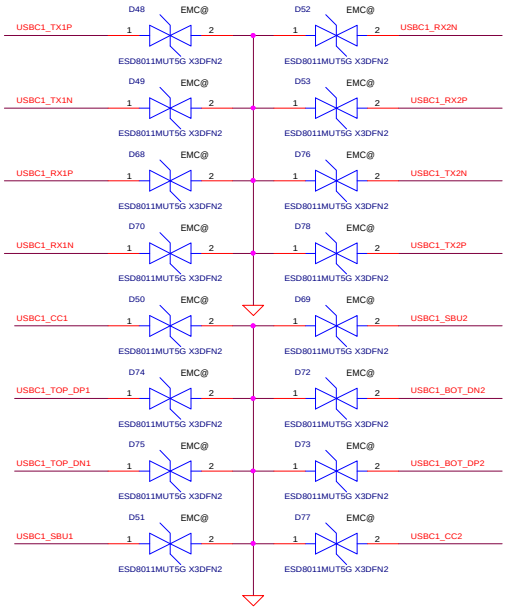
turn part EVT only
DX07SA24XJ2R1000

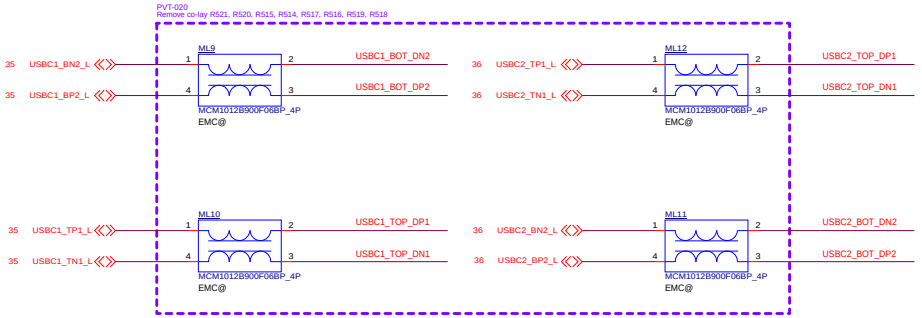


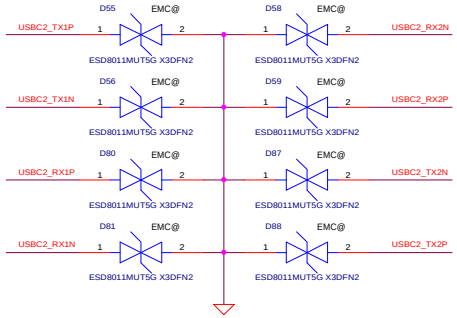
turn part EVT only
DX07SA24XJ2R1000

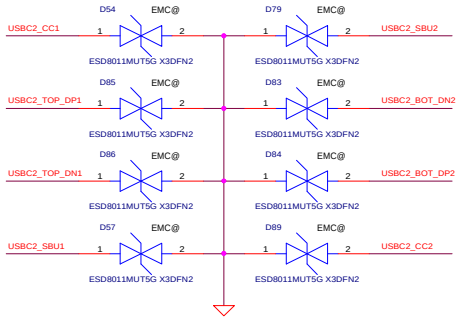


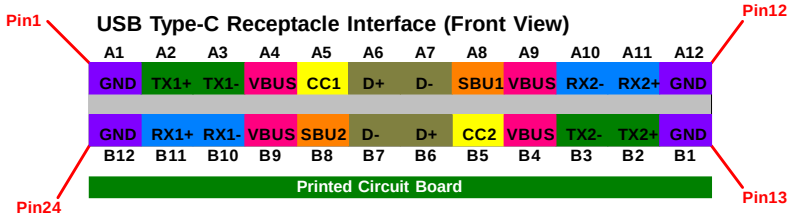


PVT-020
Remove co-lay R521, R520, R515, R514, R517, R516, R519, R518









Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P40-TYPE-C USBC1/2**

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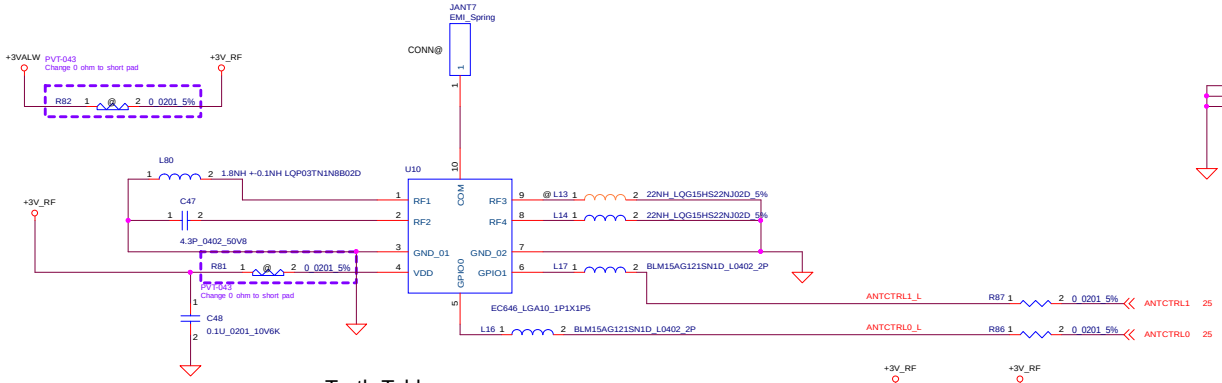
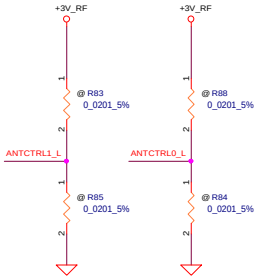
Tunnable IC

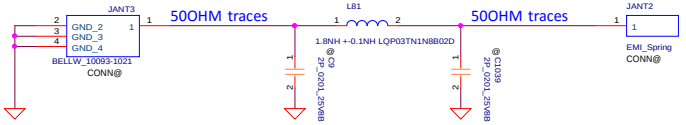


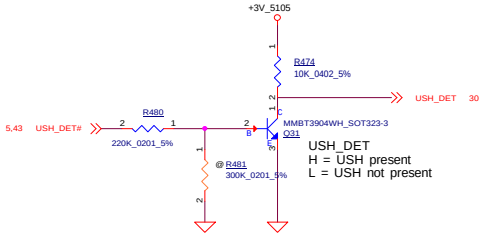
Truth Table

GPIO0	GPIO0	RF1	RF2	RF3	RF4
L	L	ON	OFF	OFF	OFF
L	H	OFF	ON	OFF	OFF
H	L	OFF	OFF	ON	OFF
H	H	OFF	OFF	OFF	ON



RF conn for WWAN





Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P41-RF Tunable IC / I/O Expander**

Size	Document Number	Rev
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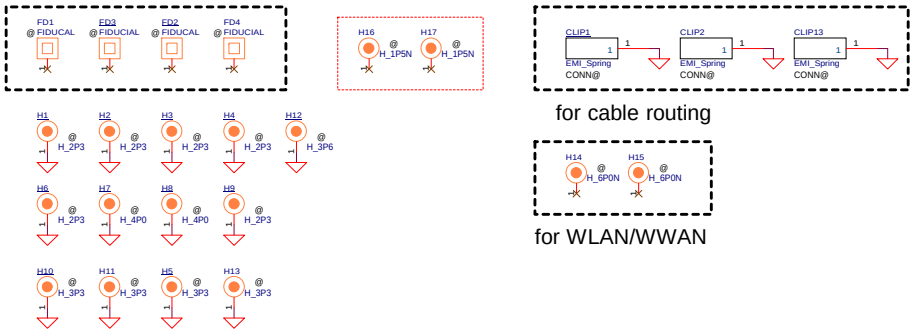
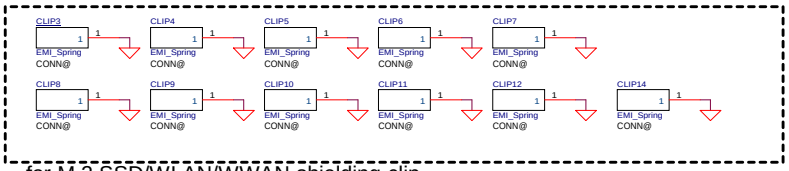
SCREW HOLE

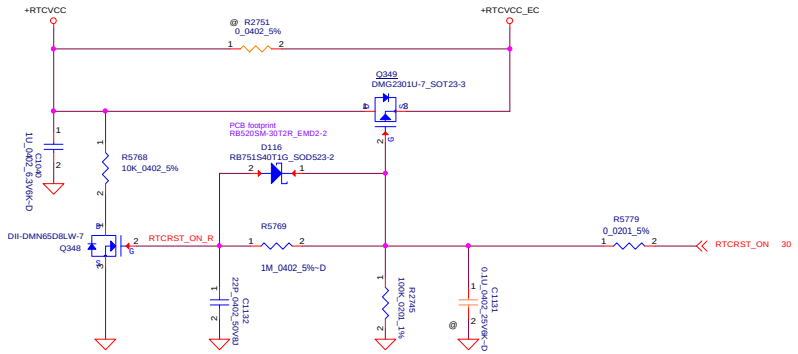


for cable routing

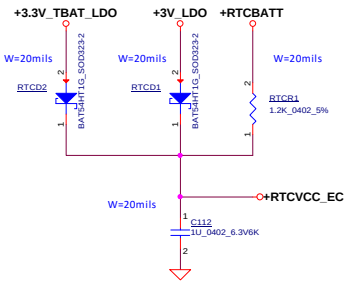
for WLAN/WWAN

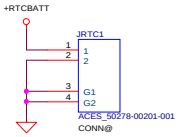


for M.2 SSD/WLAN/WWAN shielding clip

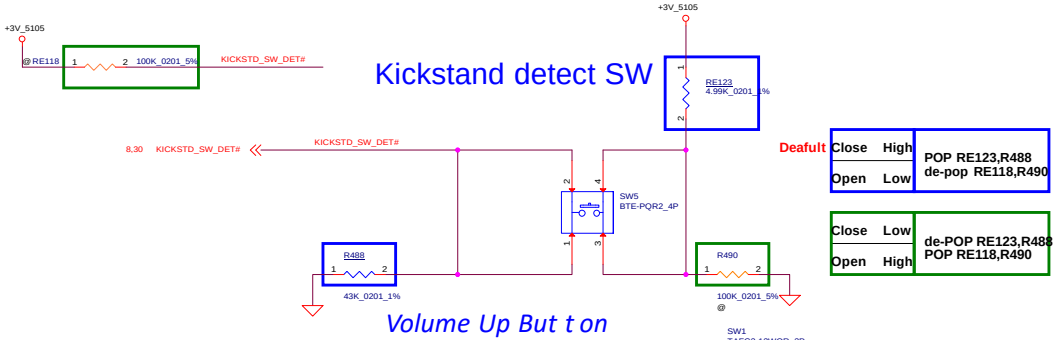


RTC





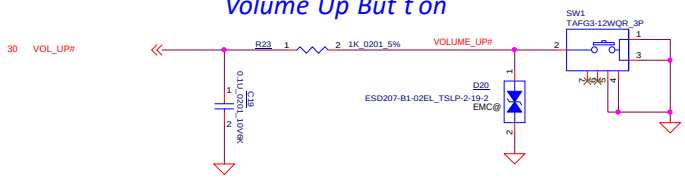
Kickstand detect SW



Deafult		
Close	High	POP RE123,R488 de-pop RE118,R490
Open	Low	

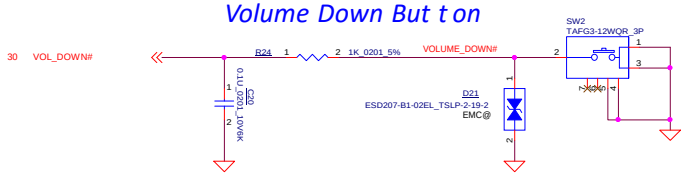
Close	Low	de-POP RE123,R488 POP RE118,R490
Open	High	

Volume Up But t on



PU 10K resistor locate on EC side

Volume Down But t on



SATA LED

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **P42-RTC, VOL SW, SCREWH**

Size	Document Number	Rev
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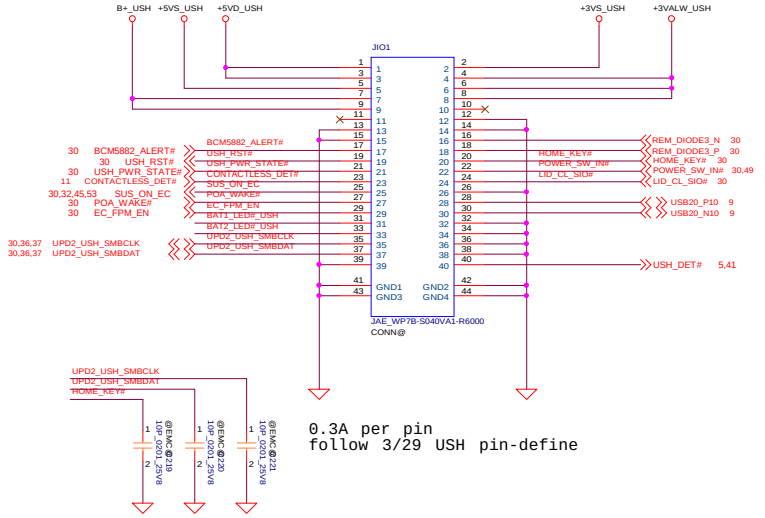
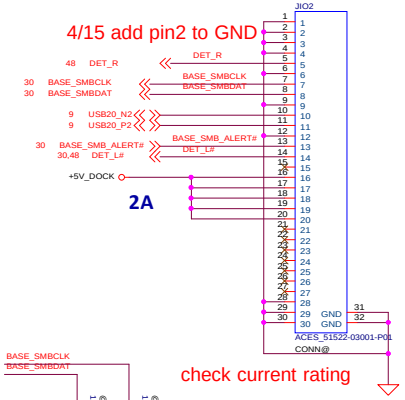
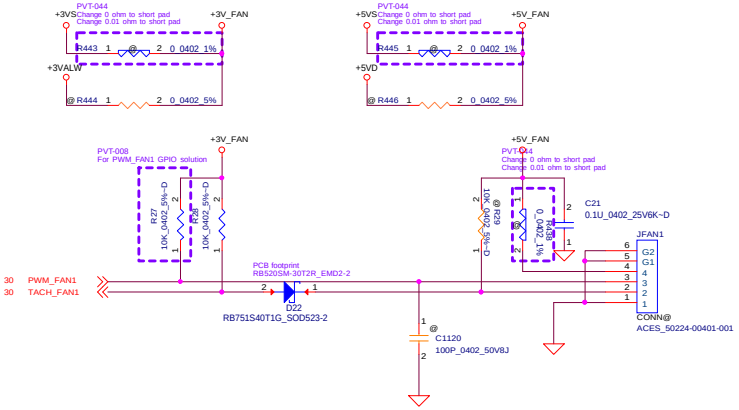
USH CONN



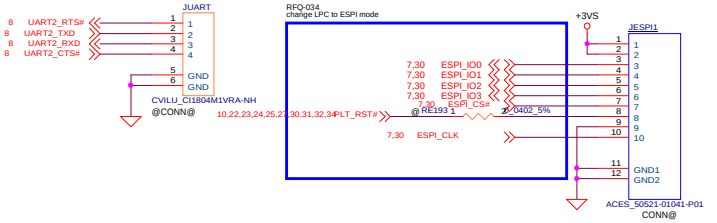
Docking CONN



FAN CONN

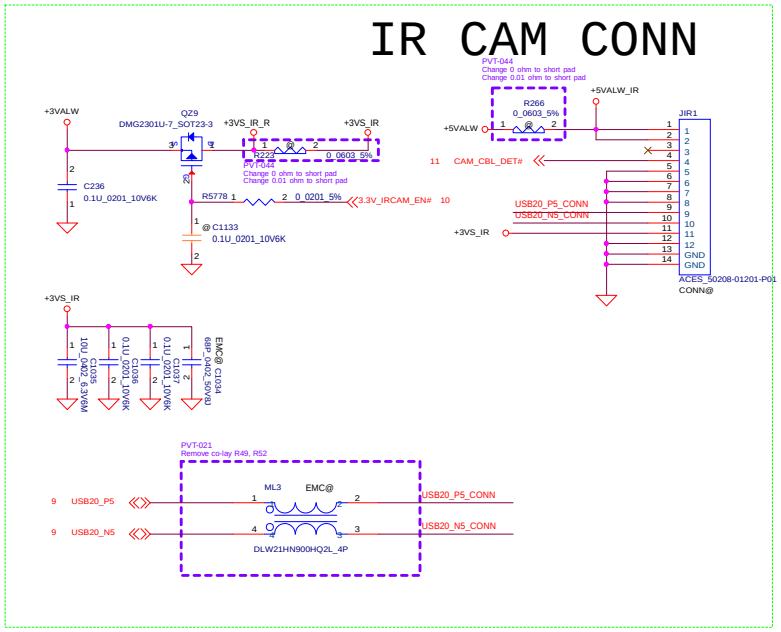


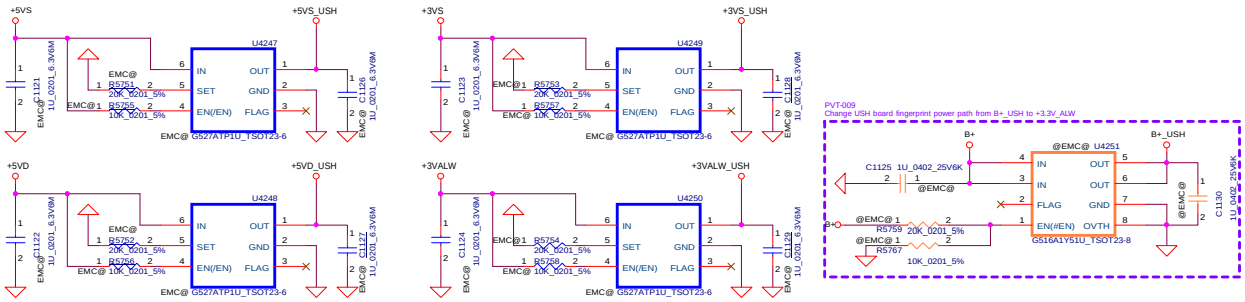
UART BIOS debug



ESPI BIOS debug

IR CAM CONN





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Issued Date	2015/10/22	Deciphered Date 2013/10/28

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Compal Electronics, Inc.

Title: **P43-IOB CONN/IR CAM**

Size	Document Number	Rev
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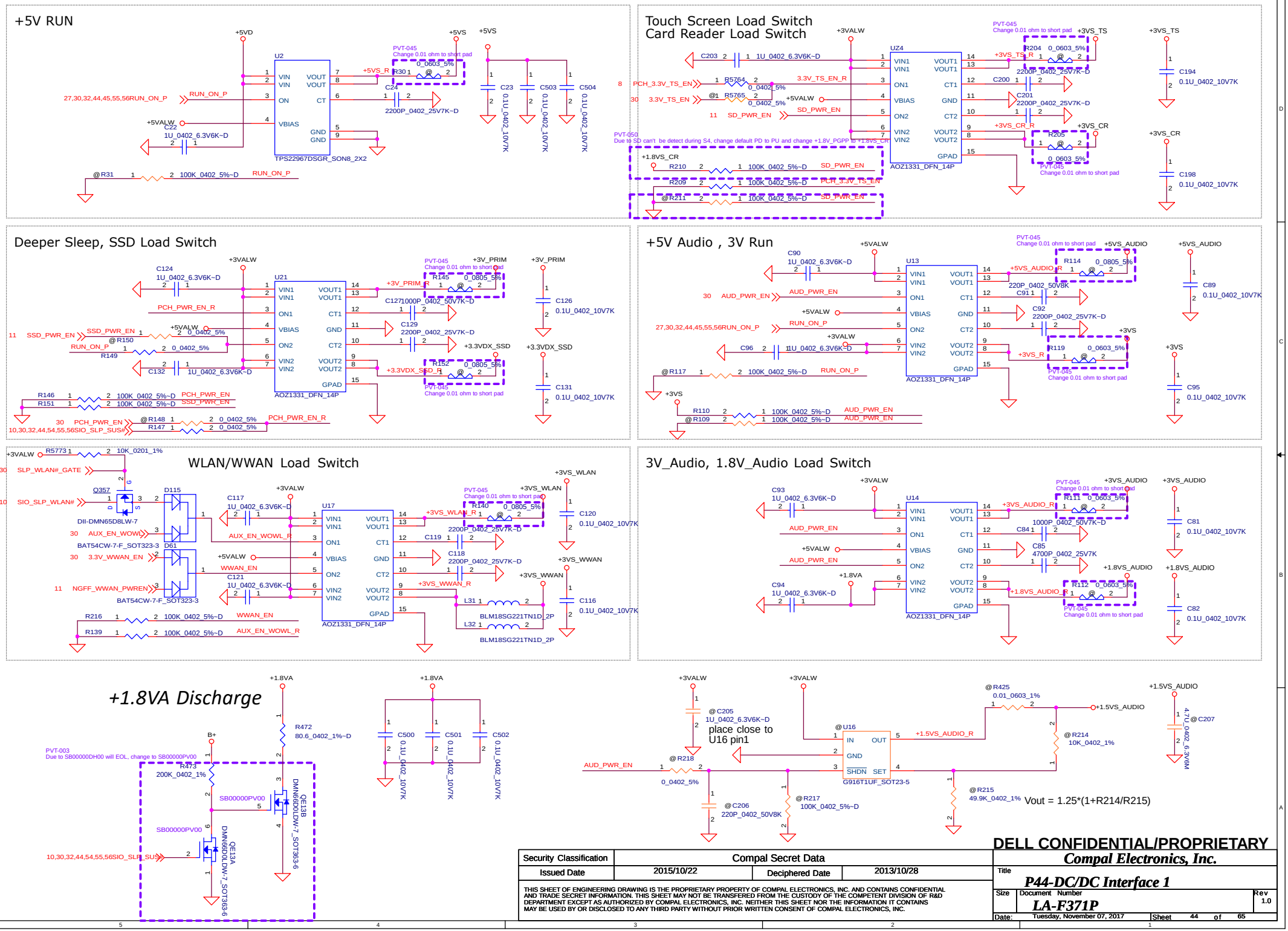

DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P44-DC/DC Interface 1

Size	Document Number	Rev
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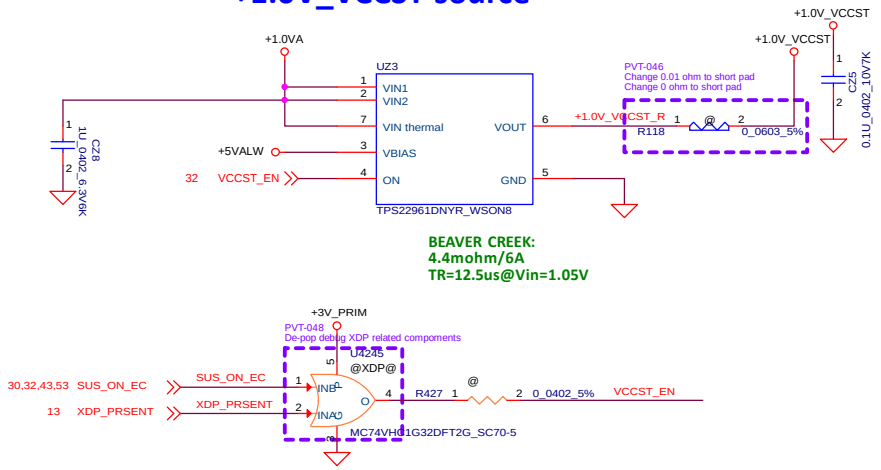
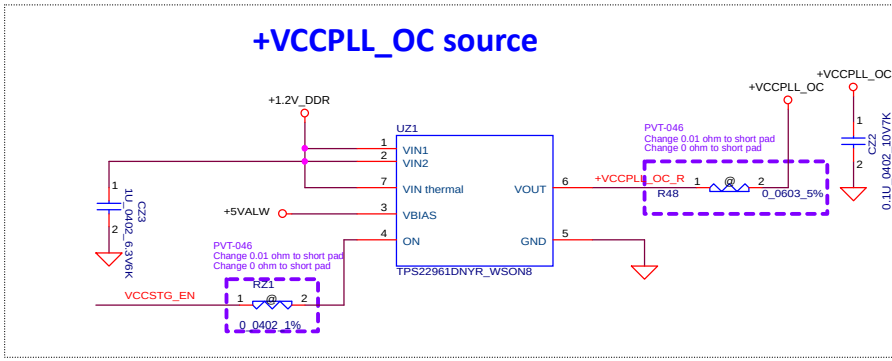
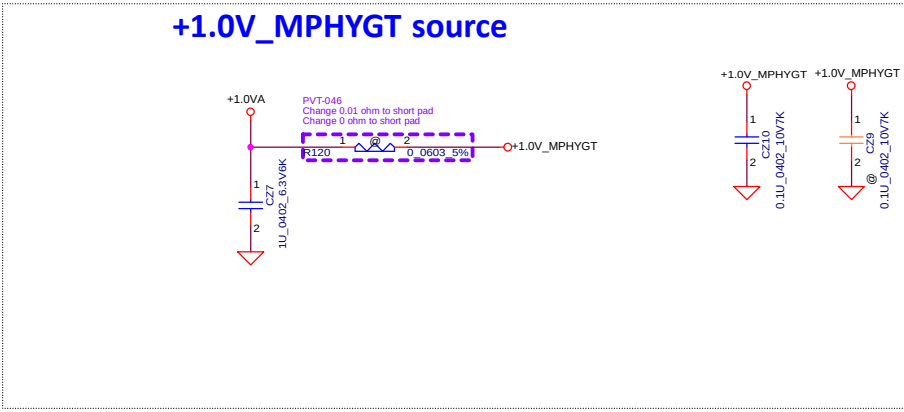
+1.0V_VCCST source



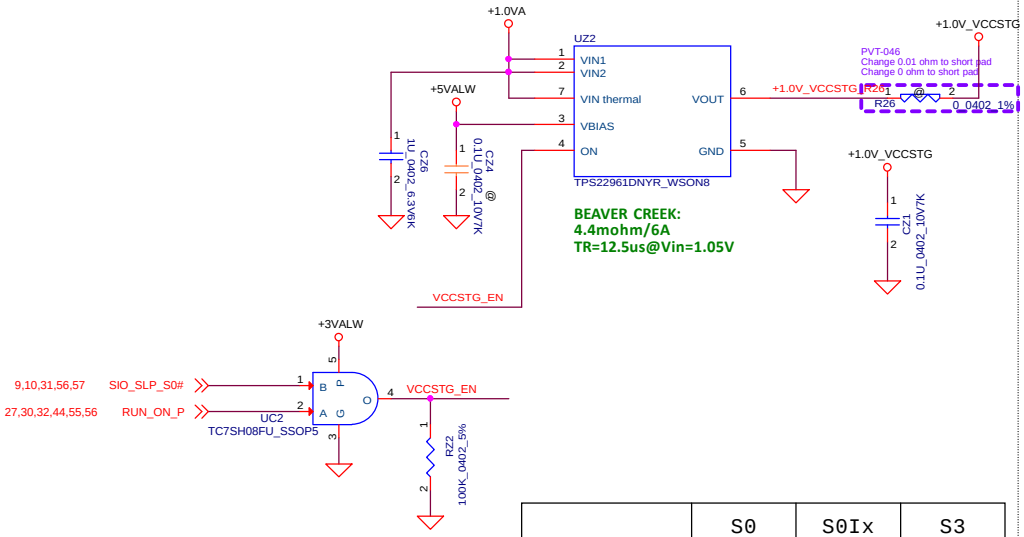
+VCCPLL_OC source



+1.0V_MPHYGT source

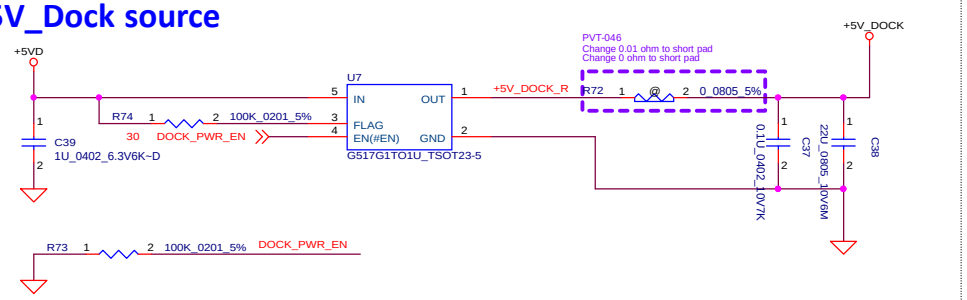


+1.0V_VCCSTG source



	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

+5V_Dock source



DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2015/10/22	Deciphered Date	2013/10/28

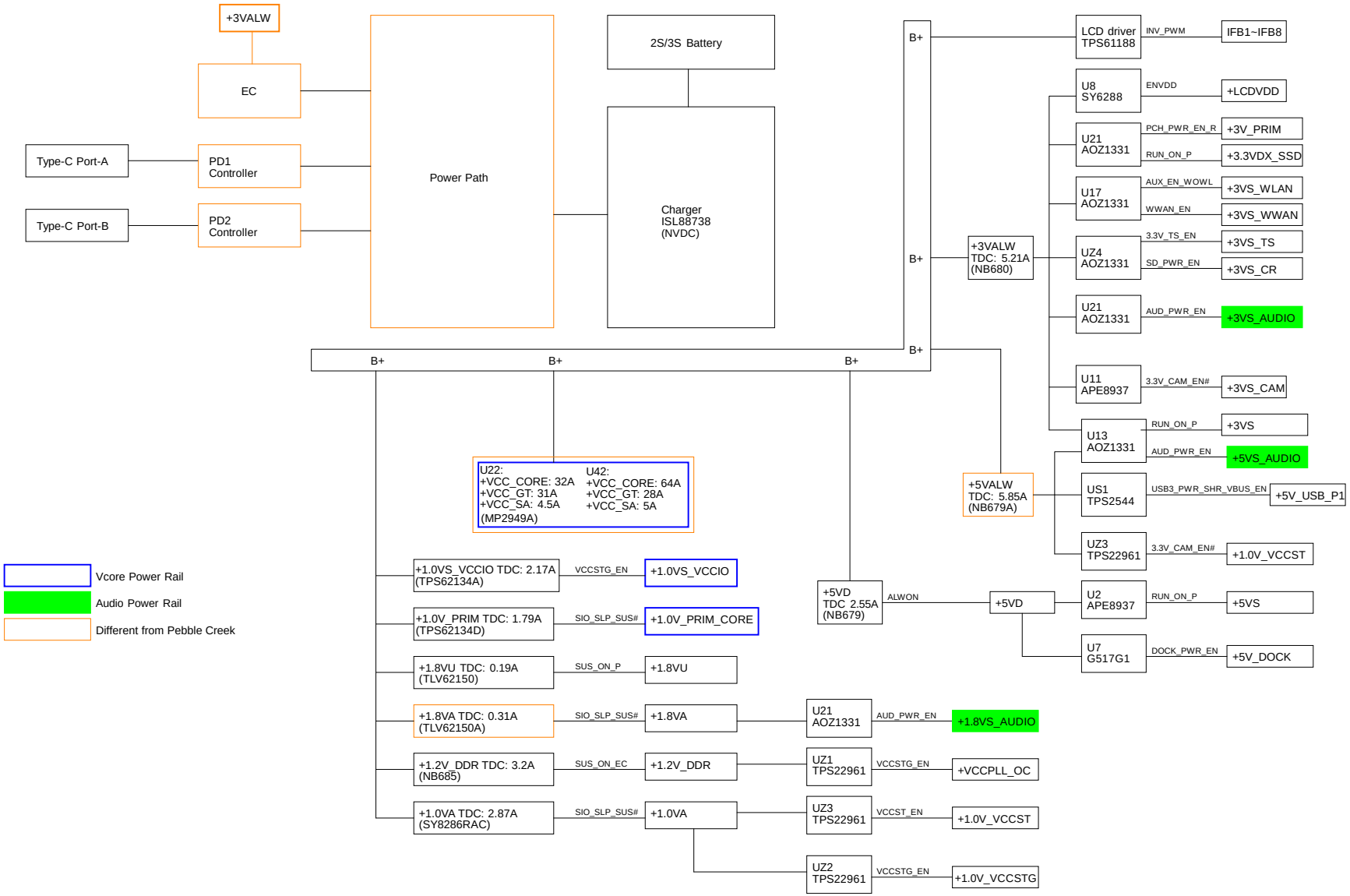
Compal Electronics, Inc.

Title: P45-DC/DC Interface 2

Size | Document Number: LA-F371P | Rev: 1.0

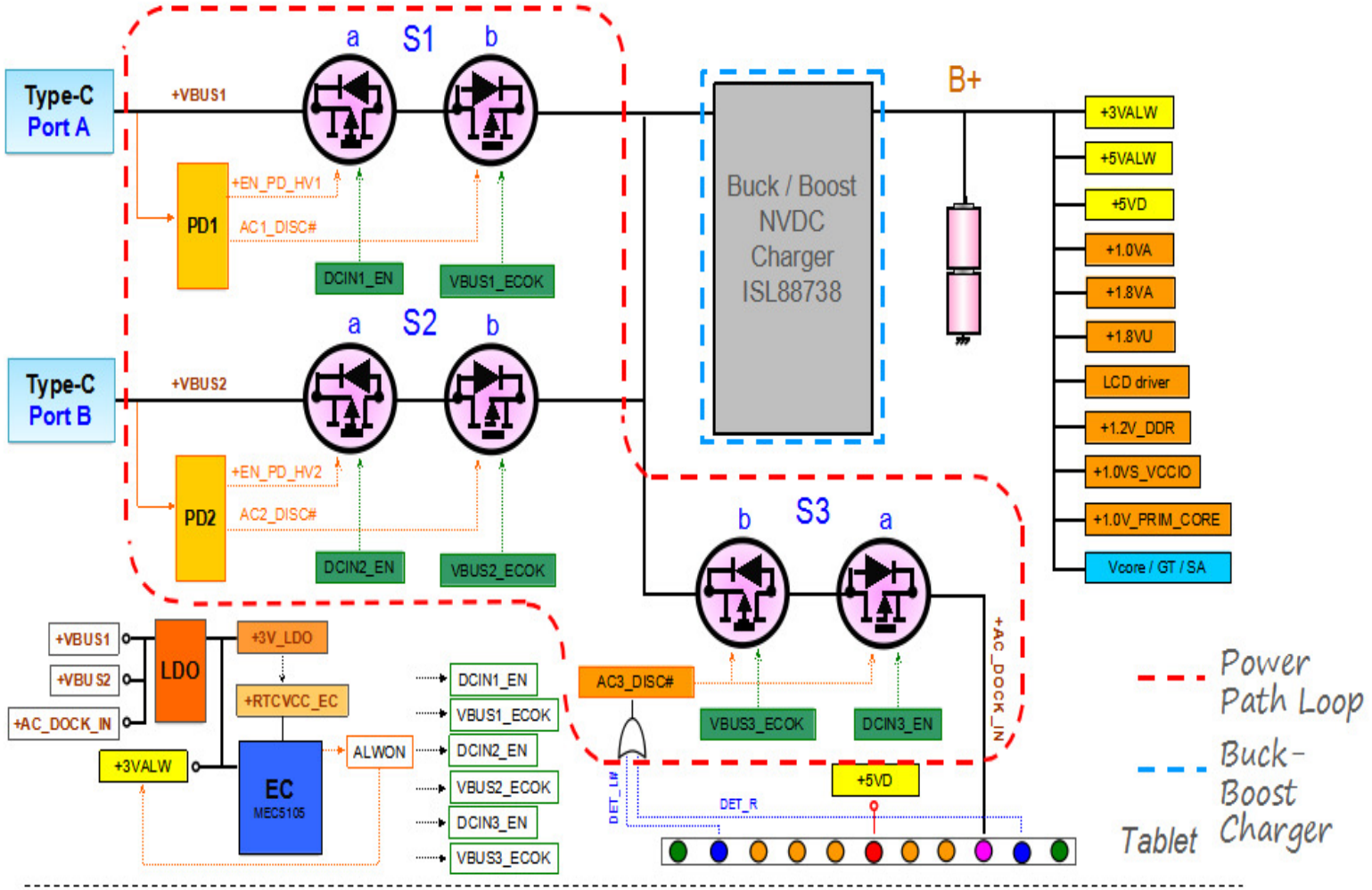
Date: Tuesday, November 07, 2017 | Sheet 45 of 65

Pebble Creek MLK Power Block - Tablet



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/08/20	Deciphered Date	2015/08/20
Title	PWR_POWER BLOCK DIAGRAM		
Size	Document Number		Rev 1.0
Date:	Tuesday, November 01, 2017	Sheet 46 of 66	

Pebble Creek MLK Power Path Block



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Issued Date	2014/08/20	Deciphered Date	2015/08/20
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			Size: Document Number: Rev: 1.0
			Date: Tuesday, November 01, 2011 Sheet 47 of 65

Function feild :
Power Path(37.1), EMC Part(47.1). 3VLDO(35.27/35.28)

Type C adapter input_1

+VBUS1_PD_20V

+VBUS1_20V

S1a

S1b

+CHG_VIN_20V

+3V_LDO

+3VALW

For MECS105

Type C adapter input_2

+VBUS2_PD_20V

+VBUS2_20V

S2a

S2b

+CHG_VIN_20V

+3V_LDO

+3VALW

For MECS105

+3.3V_LDO_PD2

+3.3V_LDO_PD1

+BATT

+BAT_TABLET

SMART Battery:
12:+BATT
11:+BATT
10:+BATT
09:+BATT
08:CLK_SMB
07:DAT_SMB
06:TBAT_3V3
05:SYS_PRES#
04:GND
03:GND
02:GND
01:GND

+3.3V_TBAT_LDO

Tablet battery 3.3V output

+CHG_VIN_20V

LCD_POWER_20V

B+

+3V_LDO

LED_SOURCE

AC_IN

LDO_IN

16.7V

2.2V

+3VALW

To EC

From Charger

To Charger

2.13V when docked

+VBUS1_20V

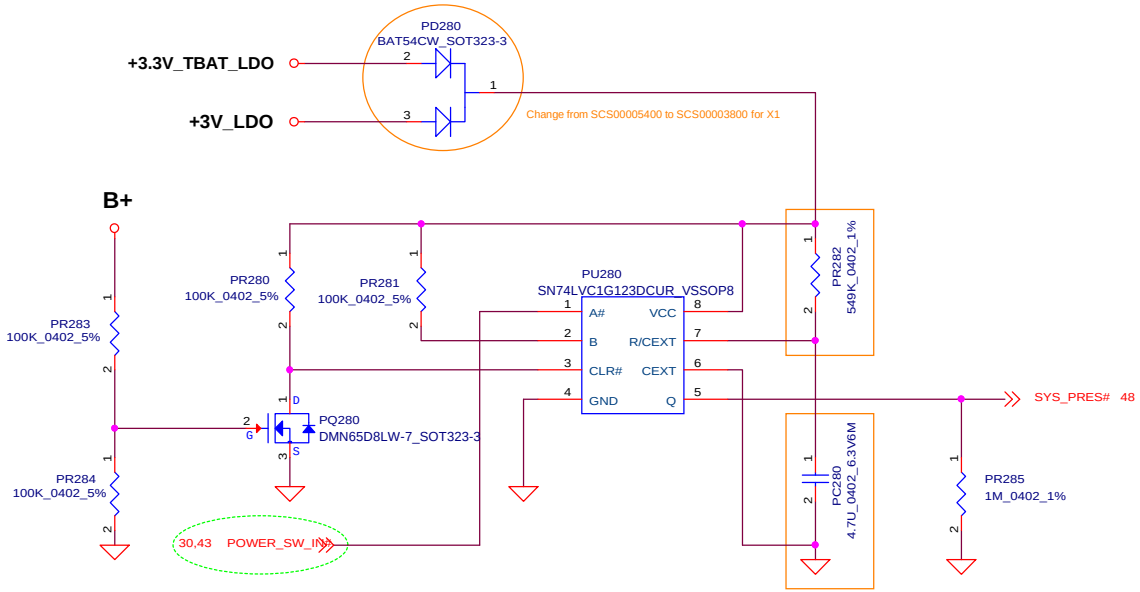
+VBUS2_20V

LDO_IN

RC delay 110ms

+3V_LDO

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/02	Deciphered Date	2013/10/28
			Title: PWR_DCIN/Power Path
			Size: LA-F371P Document Number Rev: 1.0
			Date: Tuesday, November 05, 2013 Sheet 48 of 65



FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

Security Classification	Compal Secret Data		
Issued Date	2014/08/20	Deciphered Date	2015/08/20

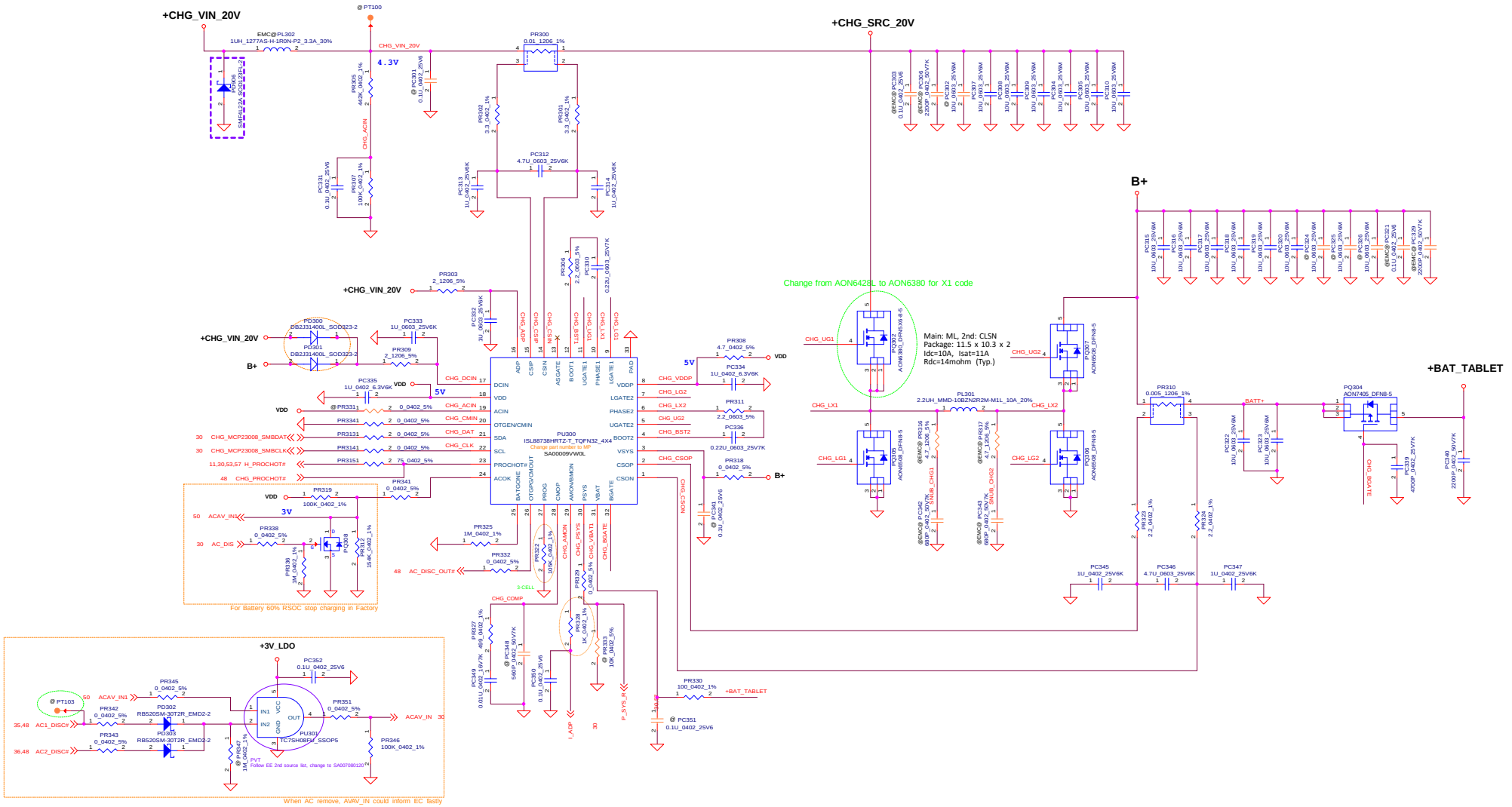
Compal Electronics, Inc.

Title: **PWR_For bat ship mode**

Size | Document Number | Rev 1.0

Date: Tuesday, November 07, 2017 | Sheet 49 of 65

Charger controller(40.1), Support component(40.2)



Security Classification	Compal Secret Data		
Issued Date	2014/10/24	Deciphered Date	2015/08/31

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Compal Electronics, Inc.

Title: **PWR_Charger (ISL88738)**

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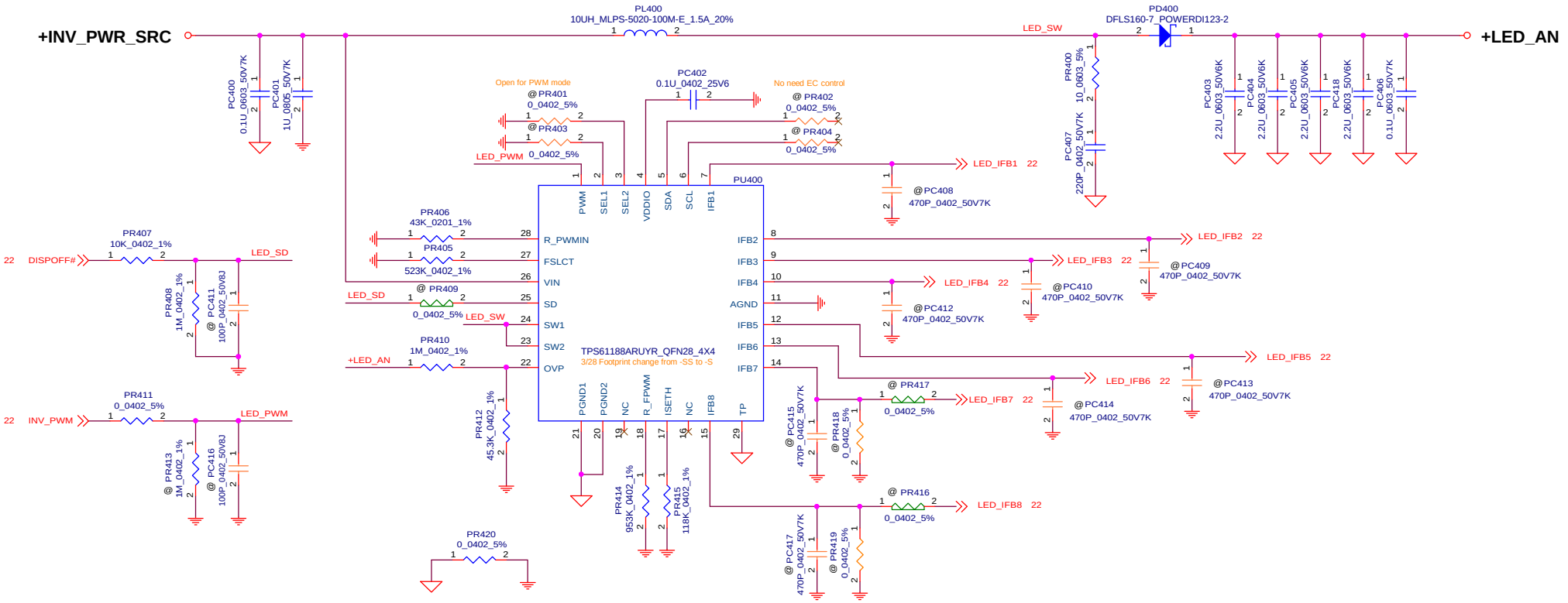
Date: Tuesday, November 07, 2017 | Sheet 50 of 65

LCD driver controller(35.31), Support component(35.32)

Current: 11.1mA x 8 = 88.8mA
Max Voltage: 6.2V x 6 = 37.2V



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

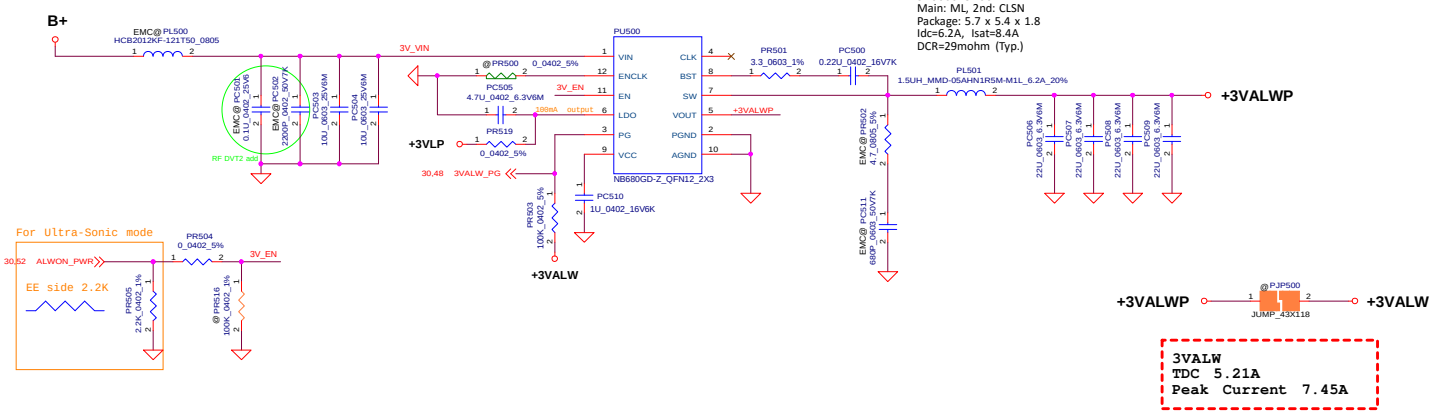
Compal Electronics, Inc.

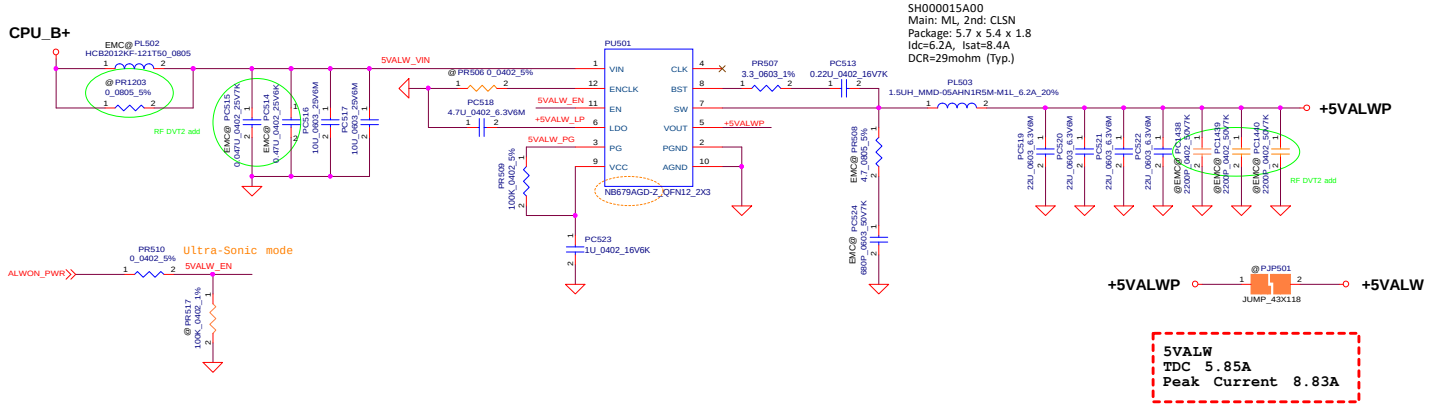
Title: PWR_LCD driver (TPS61181A)

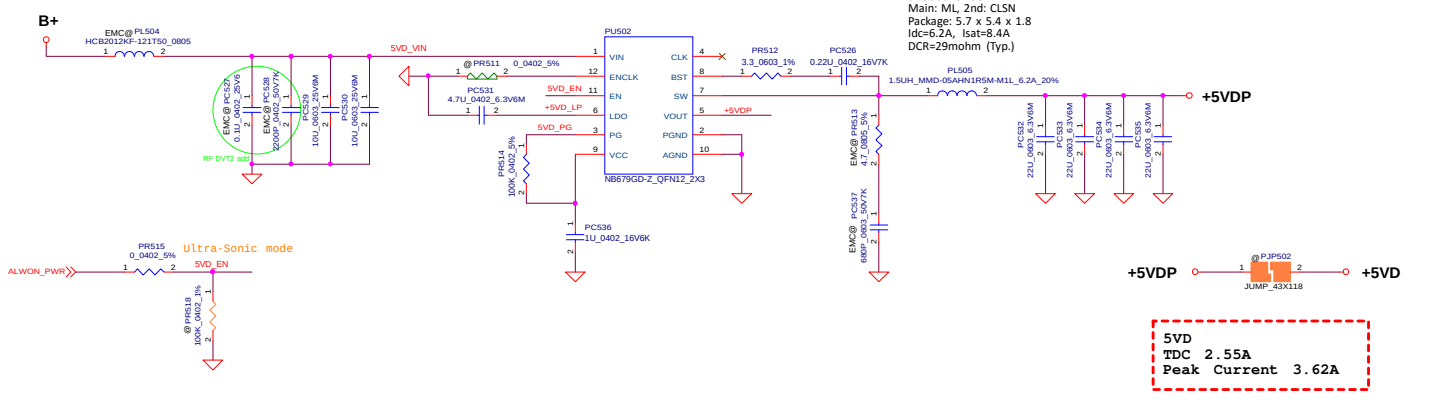
Size	Document Number	Rev
	LA-F371P	1.0

Date: Tuesday, November 07, 2017 Sheet 51 of 65

3V/5V controller(35.1), Support component(35.2)







Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: PWR_+3V(NB680)/+5V(NB679)

Size	Document Number	Rev
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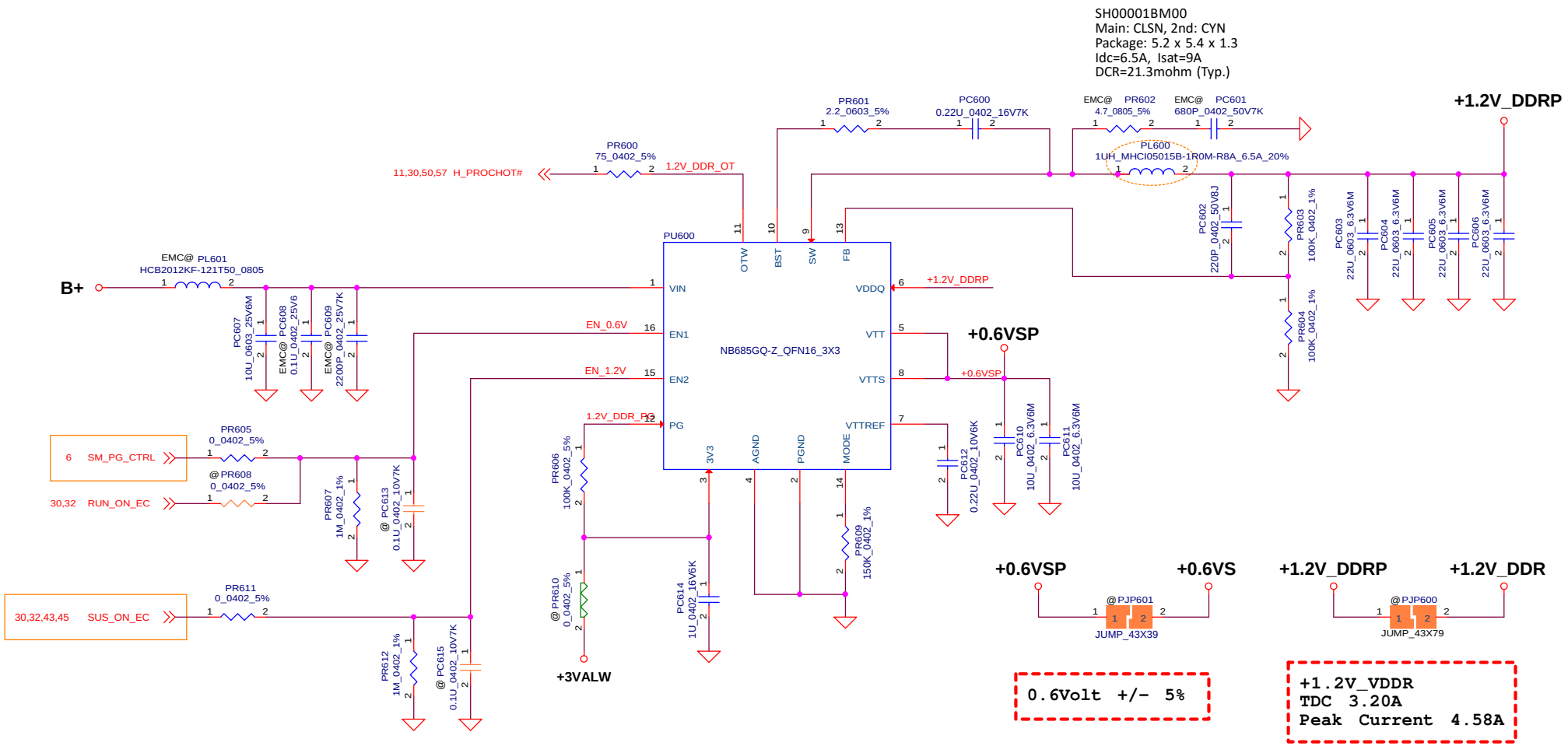
Date: Tuesday, November 07, 2017 Sheet 52 of 65

+1.2V_DDR controller(35.3), Support component(35.4)



Mode	EN1	EN2	VDDQ	VTT
S0	H	H	on	on
S3	L	H	on	off
S4/S5	L	L	off	off

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2013/04/10	Deciphered Date	2014/05/01

Compal Electronics, Inc.

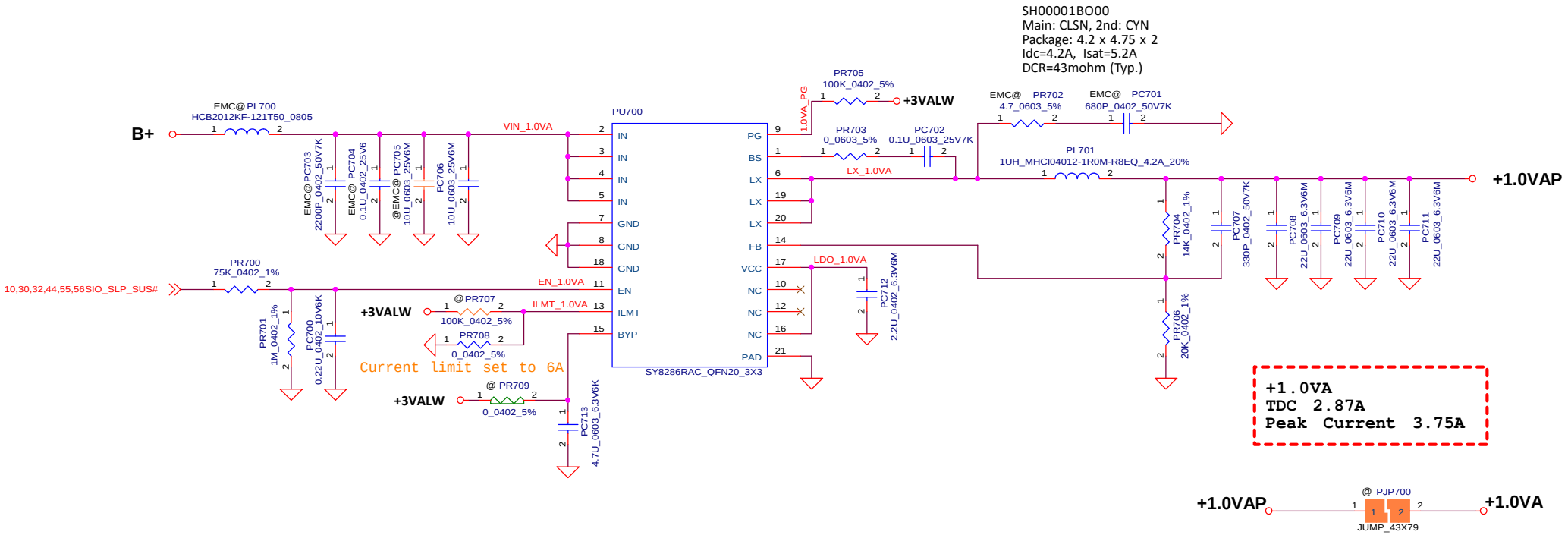
Title: PWR_+1.2V_DDR(NB685)

Size	Document Number	Rev
		1.0

Date: Tuesday, November 07, 2017 Sheet 53 of 65

Module Design

+1.0VA controller(35.5), Support component(35.6)

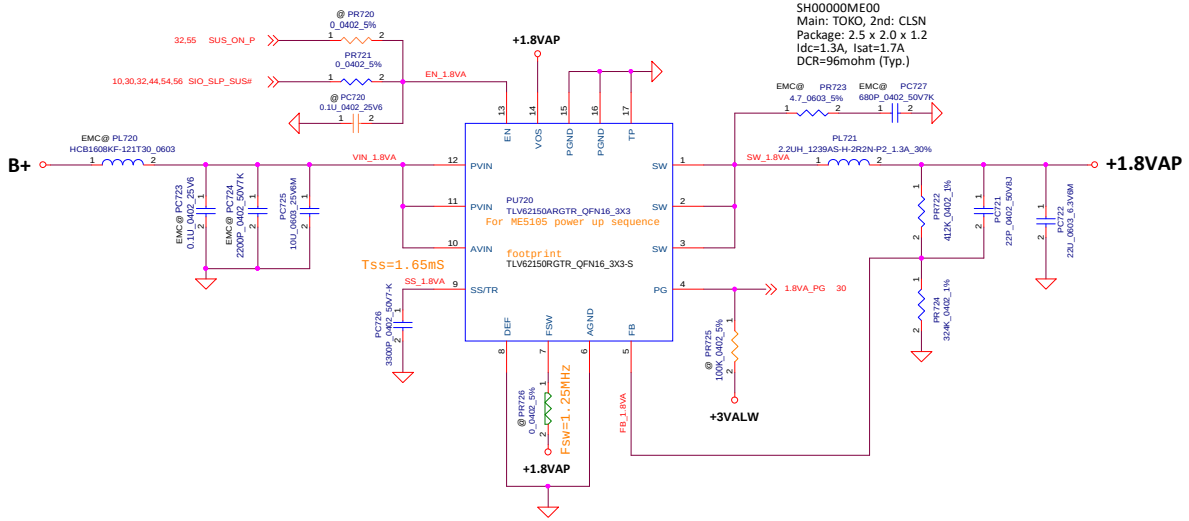


Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2014/12/05

Compal Electronics, Inc.			
Title	PWR_+1.0VA(SY8286RAC)		
Size	Document Number		Rev
	LA-F371P		1.0
Date:	Tuesday, November 07, 2017	Sheet	54 of 65

Module Design

+1.8VS controller(35.13), Support component(35.14)

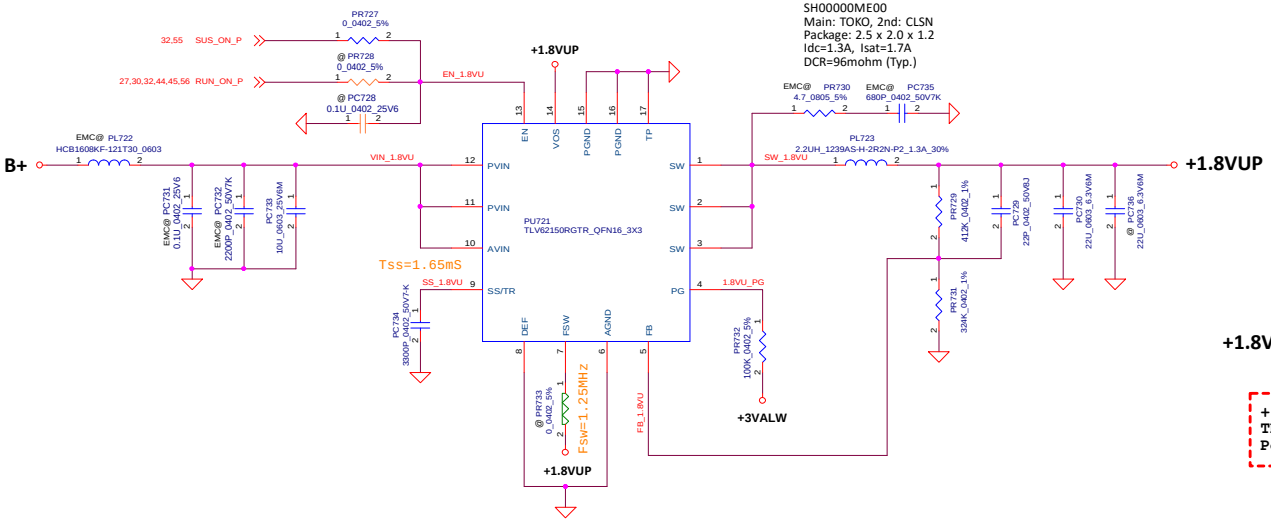


+1.8VAP → @PJP720 JUMP_43X39 → +1.8VA

+1.8VA
TDC 0.31A
Peak Current 0.45A

Module Design

+1.8VU controller(35.15), Support component(35.16)



+1.8VUP → @PJP721 JUMP_43X39 → +1.8VU

+1.8VU
TDC 0.19A
Peak Current 0.27A

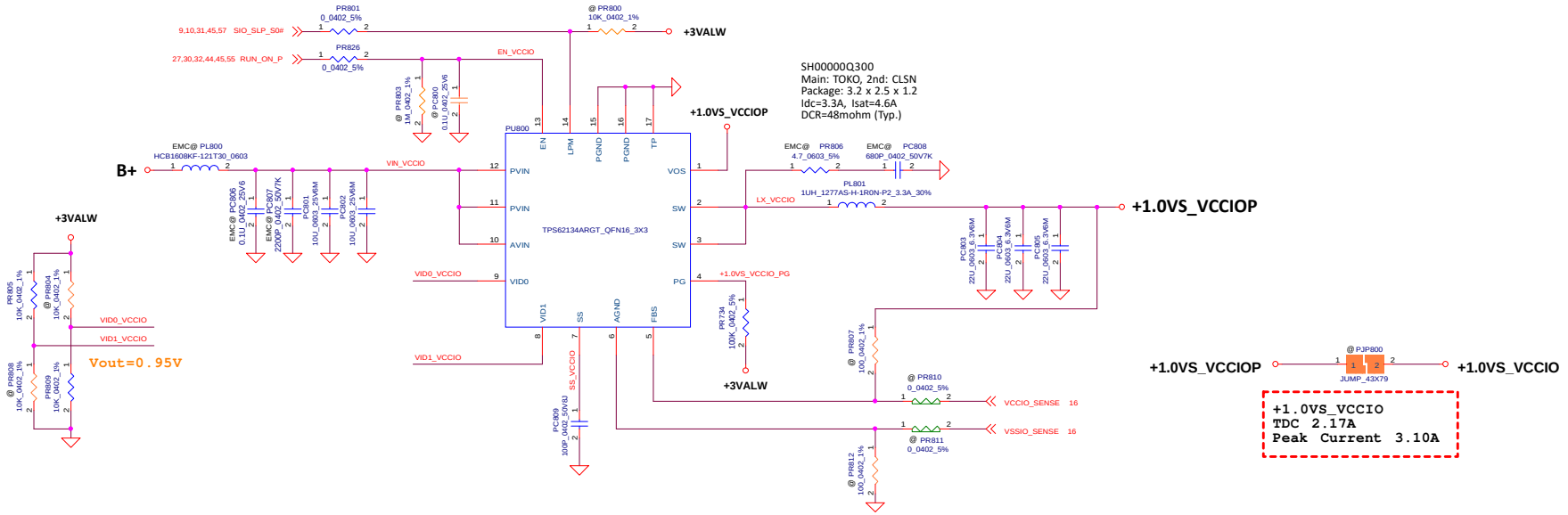
Compal Electronics, Inc.

Title: PWR_+1.8VA/+1.8VU(TLV62150)

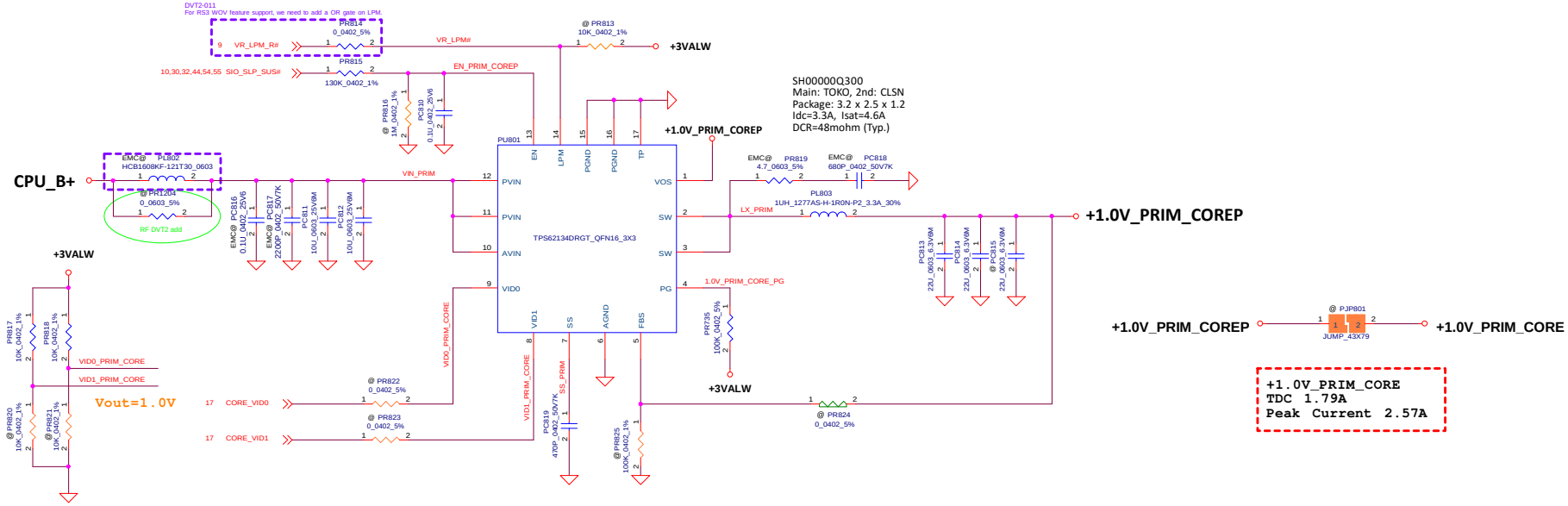
Size | Document Number: LA-F371P | Rev: 1.0

Date: Tuesday, November 07, 2017 | Sheet 55 of 65

+1.0VS_VCCIO controller(35.11), Support component(35.12)



+1.0V_PRIM_CORE controller(35.7), Support component(35.8)



Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2014/12/05

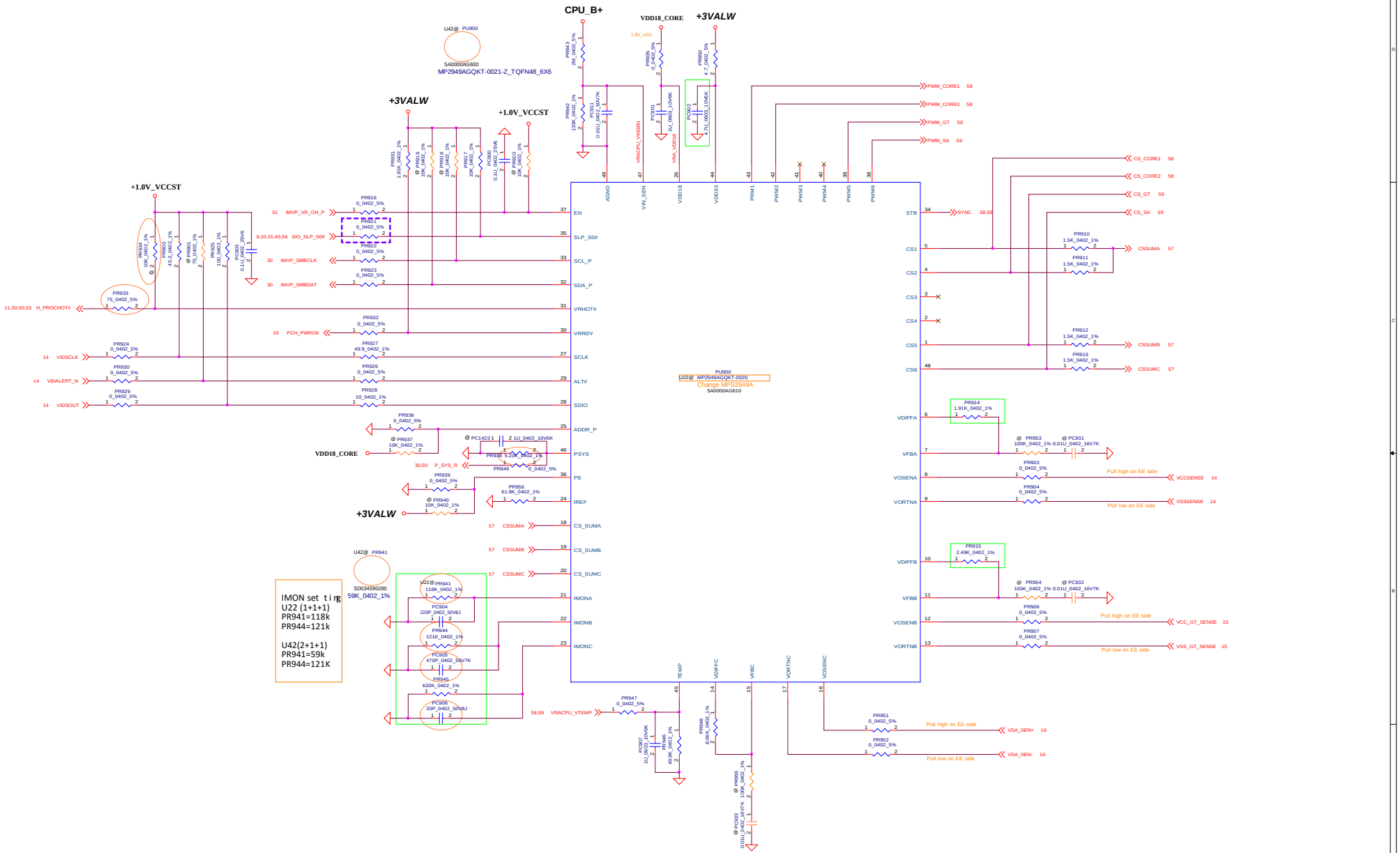
Compal Electronics, Inc.

Title: PWR_VCCIO/PRIM(TPS62134*2)

Size	Document Number	Rev
	LA-F371P	1.0

Date: Tuesday, November 07, 2017 Sheet 56 of 65

VCC_CORE controller(36.1), Drivers (36.2), Support component(36.3)



Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2014/12/05

Compal Electronics, Inc.			
Title	PWR_MP2949A		
Size	Document Number		Rev
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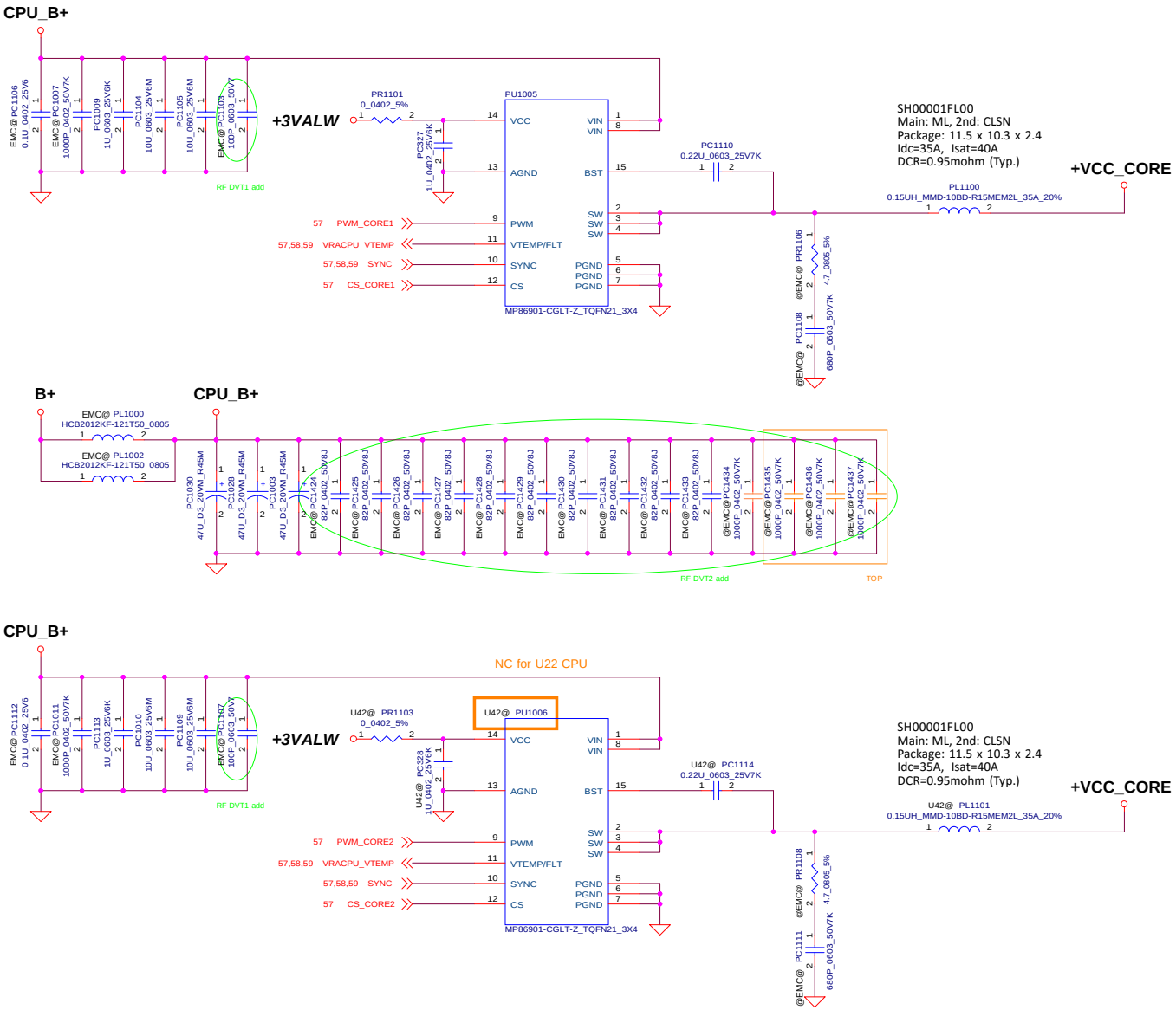
VCC_CORE Dr. MOS (36.2), Support component(36.3)



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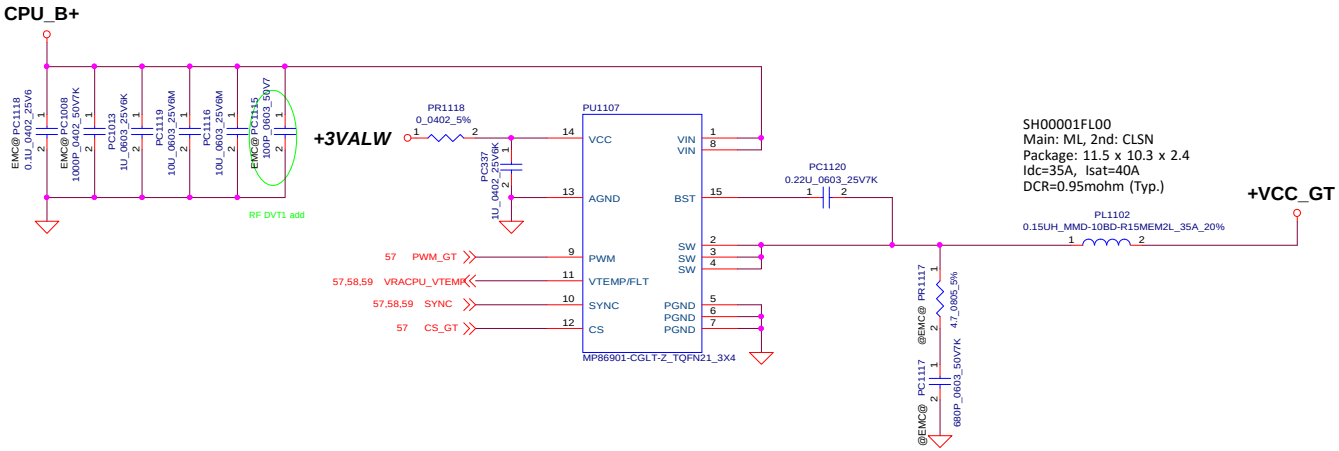
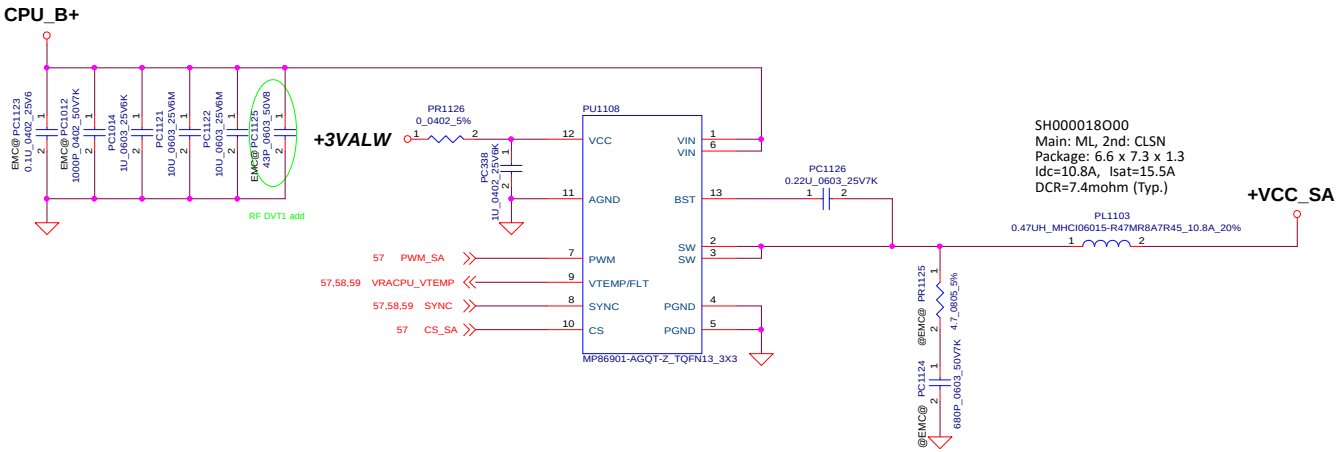
VCC_GT/SA Dr. MOS (36.2), Support component(36.3)





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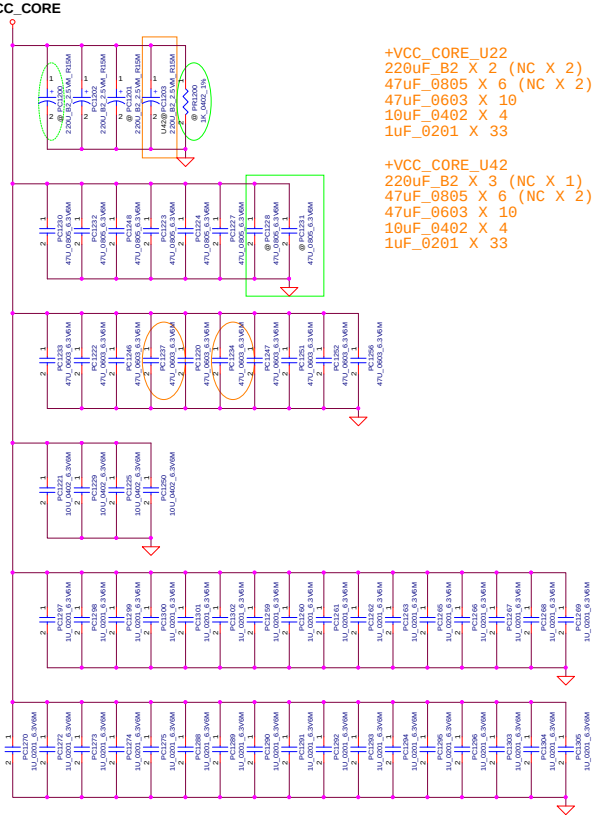
VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6), VCCIA_GT out cap(36.7)

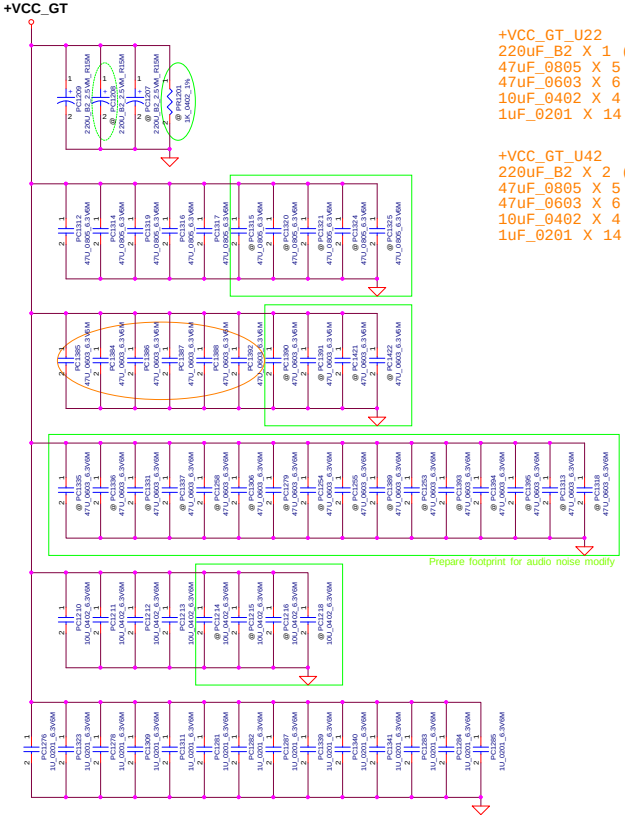
+VCC_CORE



+VCC_CORE_U22
220uF_B2 X 2 (NC X 2)
47uF_0805 X 6 (NC X 2)
47uF_0603 X 10
10uF_0402 X 4
1uF_0201 X 33

+VCC_CORE_U42
220uF_B2 X 3 (NC X 1)
47uF_0805 X 6 (NC X 2)
47uF_0603 X 10
10uF_0402 X 4
1uF_0201 X 33

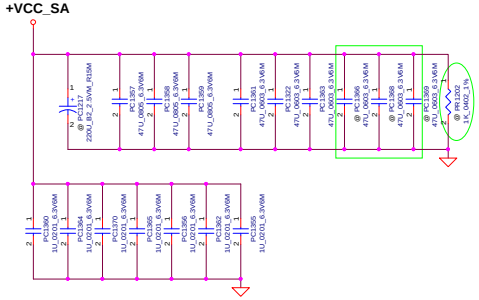
+VCC_GT



+VCC_GT_U22
220uF_B2 X 1 (NC X 2)
47uF_0805 X 5 (NC X 5)
47uF_0603 X 6 (NC X 20)
10uF_0402 X 4 (NC X 4)
1uF_0201 X 14

+VCC_GT_U42
220uF_B2 X 2 (NC X 1)
47uF_0805 X 5 (NC X 5)
47uF_0603 X 6 (NC X 20)
10uF_0402 X 4 (NC X 4)
1uF_0201 X 14

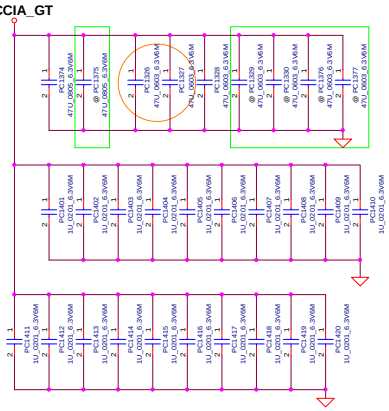
+VCC_SA



+VCC_SA_U22
220uF_B2 X 0 (NC X 1)
47uF_0805 X 3
47uF_0603 X 3 (NC X 3)
1uF_0201 X 7

+VCC_SA_U42
220uF_B2 X 0 (NC X 1)
47uF_0805 X 3
47uF_0603 X 3 (NC X 3)
1uF_0201 X 7

+VCCIA_GT



+VCCIA_GT
47uF_0805 X 1 (NC X 1)
47uF_0603 X 3 (NC X 4)
1uF_0201 X 20

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Title: **PWR-CPU DECOUPLING**

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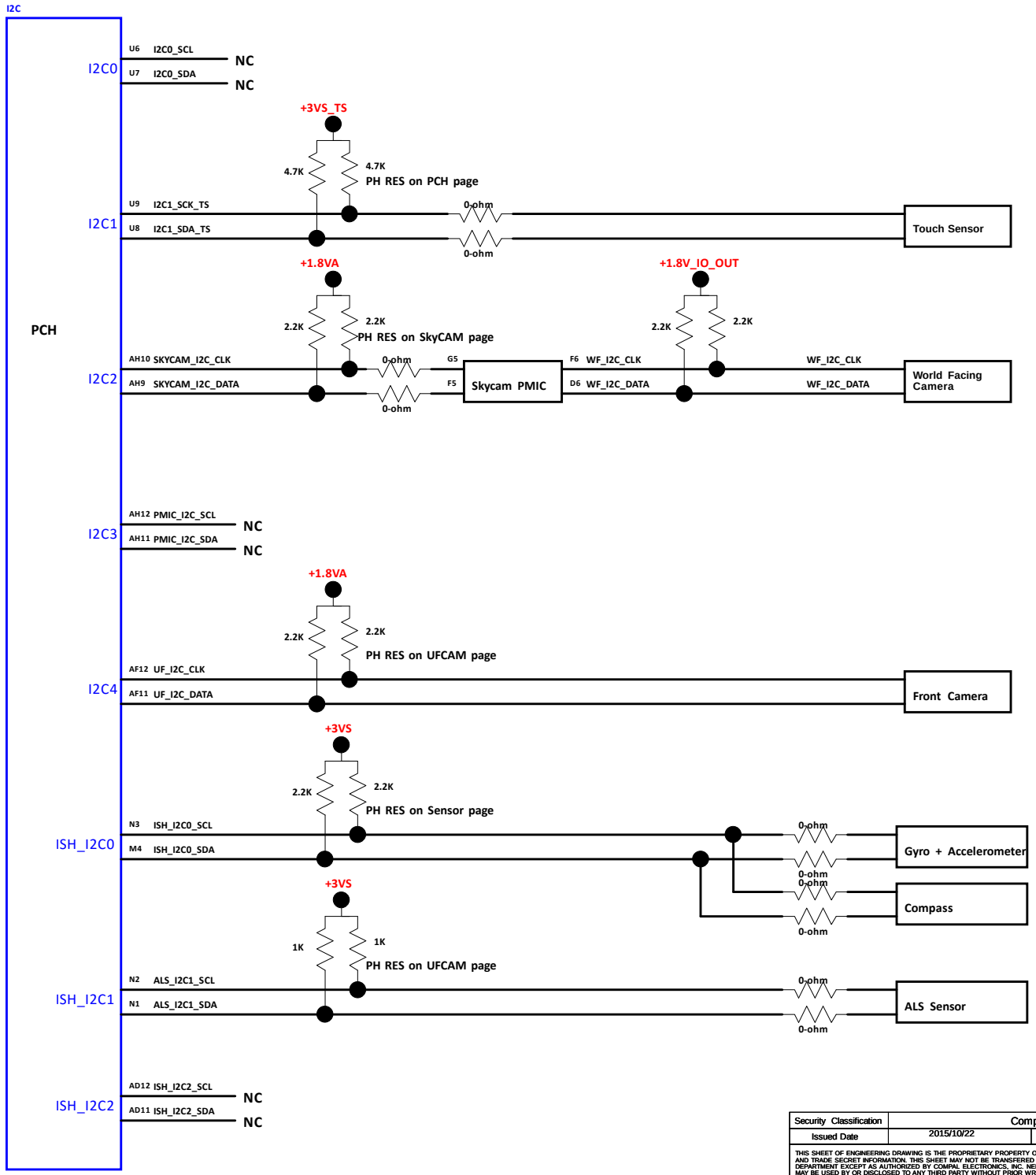

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Title: **P61-PCH I2C Block Diagram**

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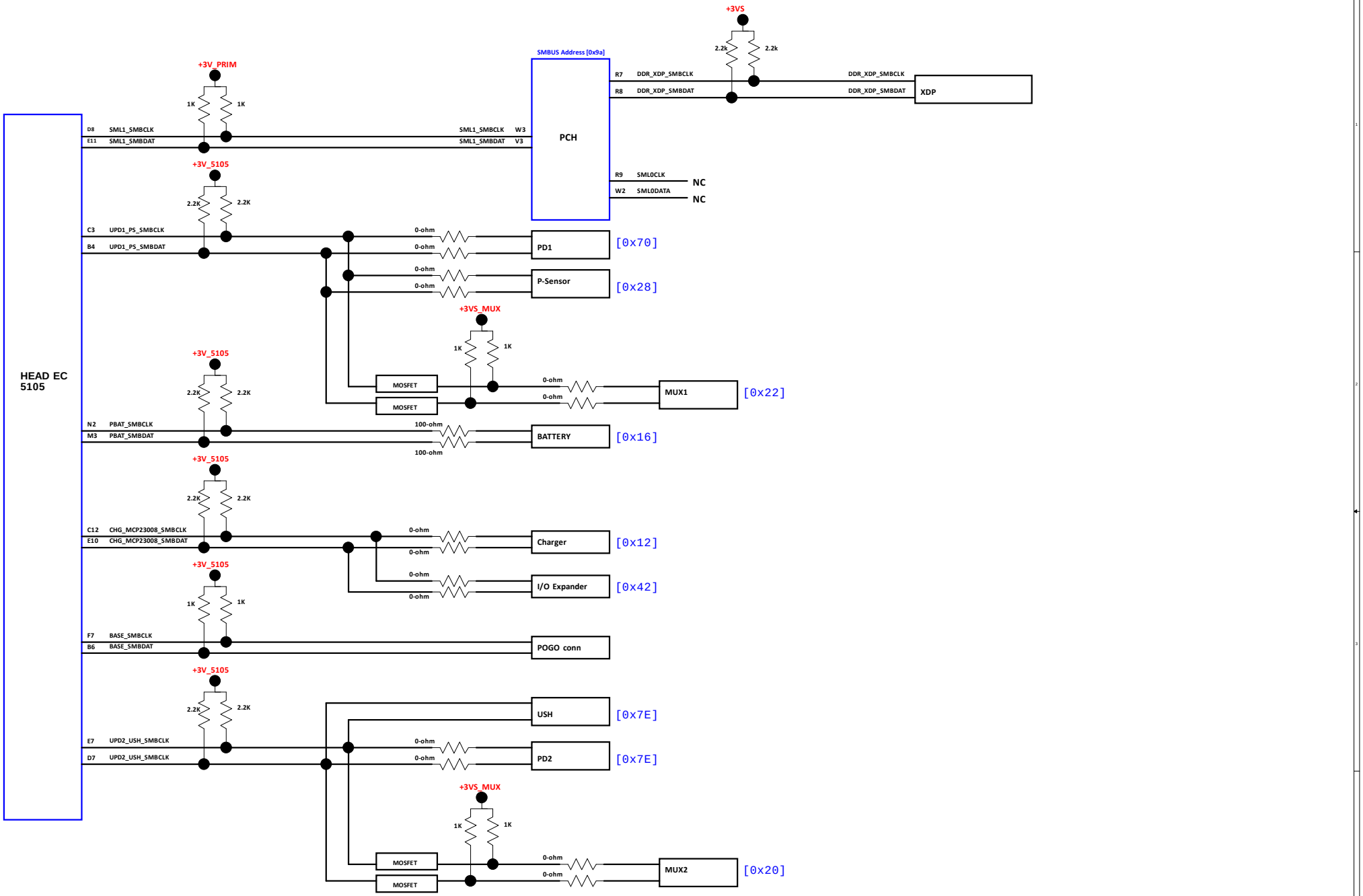

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Issued Date	2015/10/22	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	P62-SMBus Block Diagram		
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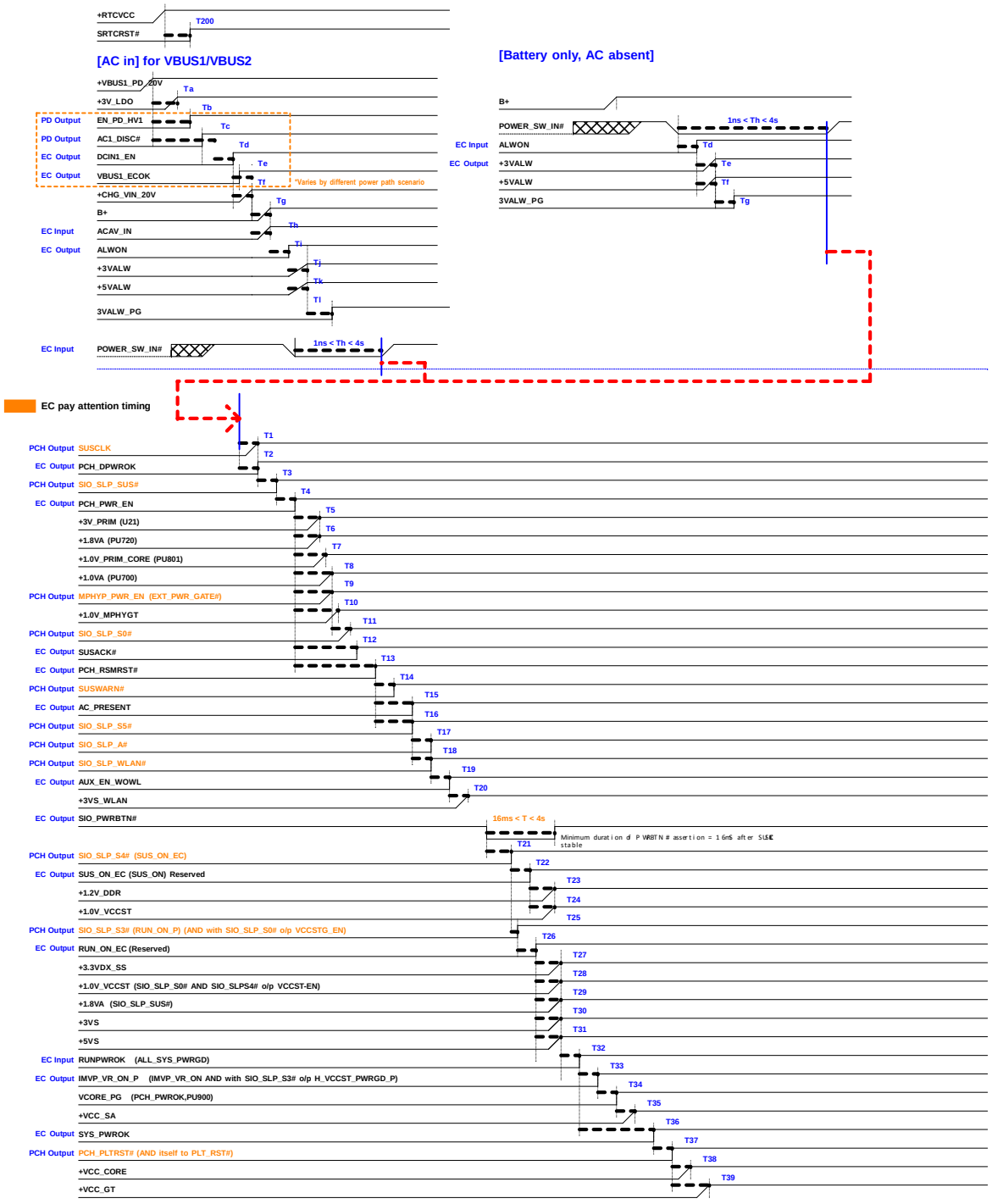
Discrete Power On Sequence



[AC in]

ITEM	Measure Point			Time
Ta	+VBUS_PD_20V	To	+3V_LDO	
Tb	3V_LDO	To	EN_PD_HV1	
Tc	EN_PD_HV1	To	AC1_DISC#	
Td	AC1_DISC#	To	DCIN1_EN	
Te	DCIN1_EN	To	VBUS1_ECOK	
Tf	VBUS1_ECOK	To	+CHG_VIN_20V	
Tg	+CHG_VIN_20V	To	B+	
Th	B+	To	ACAV_IN	
Ti	ACAV_IN	To	ALWON	
Tj	ALWON	To	+3VALW	
Tk	+3VALW	To	+5VALW	
Tl	+5VALW	To	3VALW_PG	

[Battery only, AC absent]

ITEM	Measure Point			Time
		To		
		To		
Tc	B+	To	+3V_LDO	
Th	POWER_SW_IN#		Low pluse width	
Td	POWER_SW_IN#	To	ALWON	
Te	ALWON	To	+3VALW	
Tf	ALWON	To	+5VALW	
Tg	+3VALW	To	3VALW_PG	

ITEM	Measure Point			Time
T1	DSW_ON	To	+3VALW_DSW	
T2	+3VALW_DSW	To	SUSCLK	
T3	+3VALW_DSW	To	PCH_DPWROK	
T4	PCH_DPWROK	To	SIO_SLP_SUS#	
T5	SIO_SLP_SUS#	To	PCH_PWR_EN	
T6	PCH_PWR_EN	To	+3V_PRIM	
T7	PCH_PWR_EN	To	+1.8V_PRIM	
T8	PCH_PWR_EN	To	+0.95V_PRIM	
T9	PCH_PWR_EN	To	+1.0V_PRIM	
T10	PCH_PWR_EN	To	EXT_PWR_GATE#	
T11	PCH_PWR_EN	To	SIO_SLP_S0#	
T12	EXT_PWR_GATE#	To	+1.0VA_GATE	
T13	PCH_PWR_EN	To	SUSACK#	
T14	PCH_PWR_EN	To	PCH_RSMRST#	
T15	PCH_RSMRST#	To	SUSWARN#	
T16	PCH_RSMRST#	To	AC_PRESENT	
T17	PCH_RSMRST#	To	SIO_SLP_S5#	
T18	SIO_SLP_S5#	To	SIO_SLP_A#	
T19	SIO_SLP_S5#	To	SIO_SLP_WLAN#	
T20	SIO_SLP_WLAN#	To	AUX_EN_WOWL	
T21	AUX_EN_WOWL	To	+3VS_WLAN	
T22	SIO_PWRBTN#	To	SIO_SLP_S4#	
T23	SIO_SLP_S4#	To	SUS_ON_EC	
T24	SUS_ON_EC	To	+1.8V_MEM	
T25	SUS_ON_EC	To	+1.2V_DDR	
T26	SUS_ON_EC	To	+1.0V_VCCST	
T27	SIO_SLP_S4#	To	SIO_SLP_S3#	
T28	SIO_SLP_S3#	To	RUN_ON_EC	
T29	RUN_ON_EC	To	+0.85VS_VCCIO	
T30	RUN_ON_EC	To	+1.0V_VCCSTG	
T31	RUN_ON_EC	To	+1.2VS	
T32	RUN_ON_EC	To	+1.8VS	
T33	RUN_ON_EC	To	+3VS	
T34	RUN_ON_EC	To	+5VS	
T35	+3VS	To	RUNPWROK	
T36	RUNPWROK	To	VR_ON	
T37	VR_ON	To	VCORE_PG	
T38	VCORE_PG	To	+VCC_SA	
T39	VR_ON	To	SYS_PWROK	
T40	SYS_PWROK	To	PCH_PLTRST#	
T41	PCH_PLTRST#	To	+VCC_CORE	
T42	PCH_PLTRST#	To	+VCC_GT	

update

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Title: P63-Power Up Sequence

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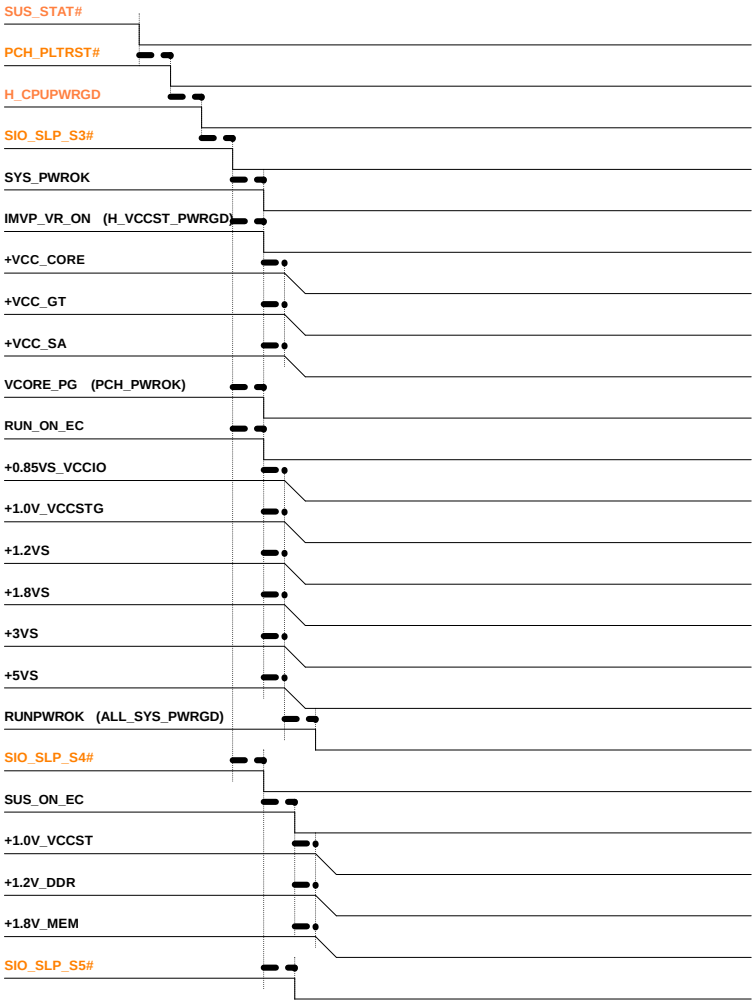

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Title: **P64-Power Down Sequence**

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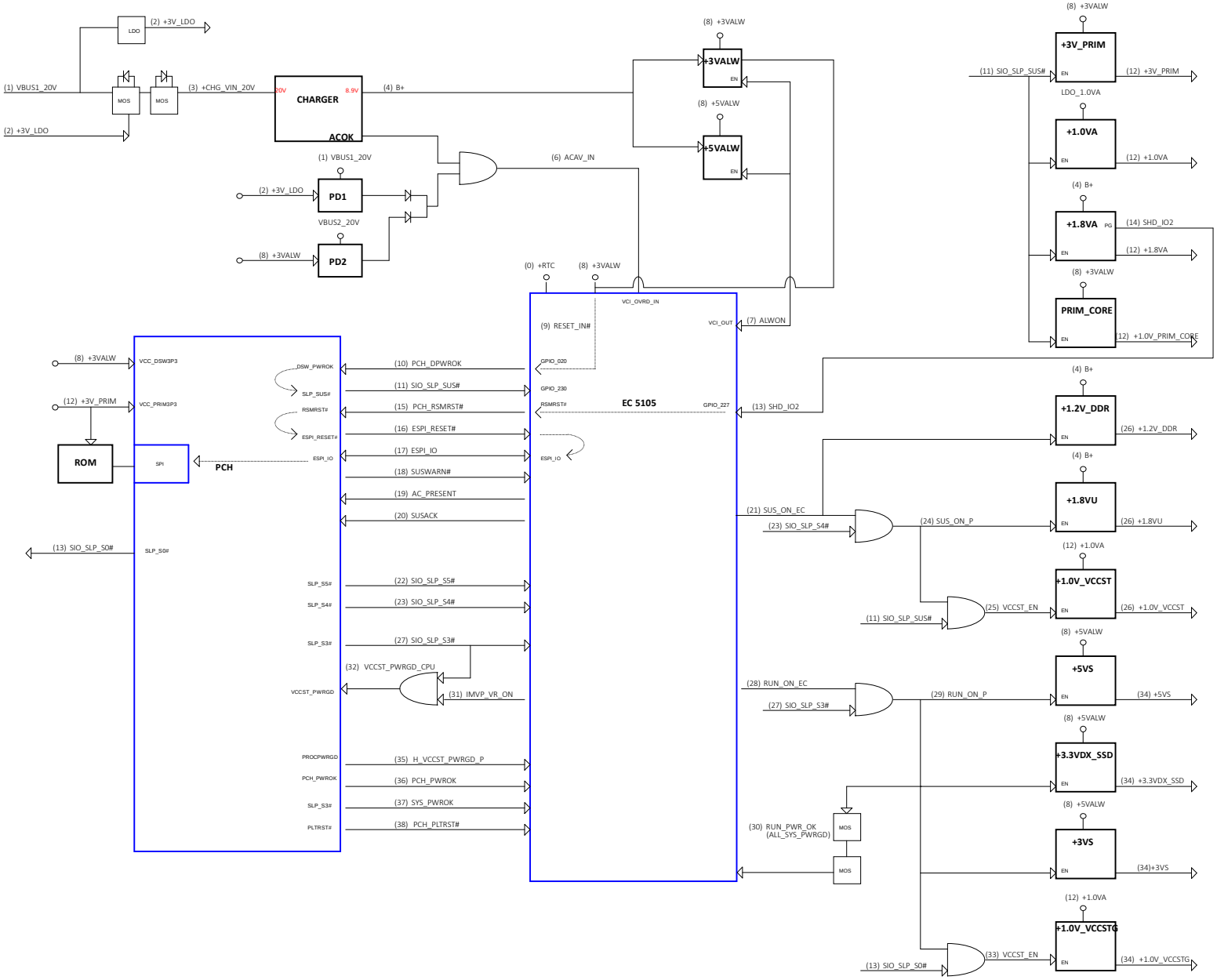

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Title: **P65-PWR Sequence Bolock Diagram**

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